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ANALYSIS AND DESIGN OF A CMOS DLL-BASED CONDITIONER FOR A SAW-DL RELATIVE HUMIDITY SENSOR

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Dedico este trabalho à minha família e aos meus amigos.

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ABSTRACT

Surface acoustic wave sensors are electromechanical structures that can be used to transduce a great variety of physical, chemical, and biological quantities into electrical quantities. The measurand interacts with the surface, usually coated with a special sensitive layer, causing variations in the energy and phase-velocity of the traveling mechanical wave. These devices behave like delay lines or resonators, altering the characteristics (phase and amplitude) of the electric signal applied to it as a function of the measurand. In the literature, these sensors are reported with high responsivity, fast response time, small size, and reasonable cost. However, the conditioners generally used to process the SAW sensor signals require large and expensive measurement equipments such as vector network analyzers, spectrum analyzer, or frequency counters. In this work, we present a novel conditioner for SAW delay line sensors. This conditioner avoid the use of such equipments, because it directly converts the measurand into a digital word. A fully-digital Delay-Locked Loop is used to measure delay variations in the signal transpassing the SAW delay line sensor. As a case study we designed an integrated circuit prototype to condition a SAW humidity sensor. The conditioner was fabricated in technology GF CMOS 130 nm, and occupies an area of 0.433 mm^2. Except for two comparators, the integrated circuit is entirely composed of standard logic circuits. This conditioner was tested stand-alone and in the proposed setup to measure relative humidity. Four saturated saline solutions were used to create four environments with specific relative humidities in the range from 32.8 to 90 %. The setup was tested in these four RH points, and the results show four distinguishable levels in the conditioner response. These results were replicated several times with a fair reproducibility. Based on these measurements, we were able to demonstrate the correct operation of the novel conditioner for SAW-DL sensors proposed in this work.

Keywords: SAW sensor, Delay-Locked Loop, relative humidity, CMOS.

RESUMO

Sensores por onda acústica de superfície são estruturas eletromecânicas que podem ser utilizadas na transdução de uma ampla variedade de grandezas físicas, químicas, e biológicas para variáveis elétricas. A grandeza a ser convertida interage com a superfície, usualmente coberta com um filme sensível, causando variações na energia e velocidade de fase da onda mecânica. Estes dispositivos se comportam como linhas de atraso ou ressonadores, alterando as características (fase e amplitude) do sinal elétrico aplicado em função da grandeza. Na literatura, estes sensores são reportados com alta sensibilidade, rápida resposta, tamanho pequeno e de razoável custo. Entretanto, o condicionador geralmente utilizado para processar os sinais do sensor SAW requer equipamentos eletrônicos grandes e de alto custo, como por exemplo analisadores de rede, analisadores de espectro, ou contadores de frequência. Neste trabalho, um novo condicionador é proposto para sensores SAW (do tipo linha de atraso). Este condicionador evita o uso de tais equipamentos, pois faz uma conversão direta da grandeza a ser medida para uma palavra digital. Uma malha de travamento de atraso totalmente digital é utilizada para medir variações no atraso do sinal passando através do sensor. Como estudo de caso, projetamos um protótipo em circuito integrado deste condicionador para um sensor SAW de umidade. O condicionador foi fabricado em tecnologia GF CMOS 130 nm, e ocupa uma área de 0.433 mm^2. Exceto por dois comparadores, o condicionador é inteiramente composto por circuitos lógicos padrão. Este condicionador foi testado sozinho e dentro do setup proposto para medição de umidade. Quatro soluções salinas saturadas foram utilizadas para criar quatro ambientes com umidades relativas específicas na faixa de 32.8 a 90 %. O setup foi testado nestes quatro pontos de umidade, e os resultados mostram quatro níveis distintos na resposta do condicionador. Estes resultados foram replicados diversas vezes com razoavel reprodutibilidade. Baseando-se nestas medições, demonstramos a operação correta do novo condicionador de sinais para sensor SAW proposto neste trabalho.

Palavras-chave: Sensor SAW, malha de travamento de atraso, umidade relativa, CMOS.

RESUMO EXPANDIDO

Introdução

Sensores por onda acústica de superfície, ou simplesmente sensores SAW (do inglês *Surface Acoustic Wave*), tem sido demostrado fabricáveis em uma ampla variedade de aplicações, agindo como transdutores de grandezas físicas, químicas e biológicas para grandezas elétricas. Na literatura, estes sensores são amplamente reportados com alta responsividade, rápida resposta temporal, tamanho reduzido e razoável custo de fabricação. Porém, os condicionadores usualmente utilizados para processar os sinais destes sensores requerem equipamentos eletrônicos grandes e caros, como analisadores de rede, analisadores de espectro, e contadores de frequência. Este trabalho propõem uma nova forma de condicionar sensores SAW-DL (dispositivo SAW do tipo linha de atraso). Um sensor SAW-DL de umidade relativa é utilizado como estudo de caso. Um DLL (do inglês *Delay Locked Loop*) é utilizado para medir o atraso causado pelo sensor, que se torna sensível à umidade relativa após a deposição de um filme fino de óxido de grafeno.

Objetivos

O objetivo geral deste trabalho é desenvolver um circuito integrado para realizar o condicionamento de um sensor SAW-DL de umidade relativa desenvolvido e fabricado pelo Dr. Sergey Balashov (CTI Renato Archer).

Os objetivos específicos deste trabalho são:

- Estudar o DLL como um sistema de medição de atrasos temporais, e como isso pode ser aplicado como um condicionador de sensores SAW-DL;
- Estudar a arquitetura proposta através de uma revisão bibliográfica e de modelos matemáticos;
- Projetar um circuito integrado, com especial atenção a testabilidade do circuito;
- Medir as funcionalidades do circuito integrado isolado;
- Projetar um setup confiável para realizar a medição de umidade relativa, contendo o sensor e o circuito integrado;
- Medir umidade relativa com este setup para verificar o comportamento esperado do condicionador proposto;

Metodologia

A metodologia para atingir os objetivos propostos começou com uma revisão bibliográfica do estado da arte em sensores SAW. A partir desta revisão bibliográfica foi possível entender melhor os princípios físicos da operação do sensor. Após esta etapa, passou-se para o estudo do DLL, utilizando artigos e análise de sistemas. Uma modelagem matemática foi obtida, o que possibilitou um entendimento muito mais profundo do funcionamento do DLL, e de como utilizá-lo para condicionar os sinais do sensor. Em sequência, foi passado para a fase de projeto do circuito integrado. Nesta etapa, a arquitetura foi projetada e simulada até que atingíssemos os requisitos e funcionalidades esperados. O projeto foi então mandado para a fabricação e encapsulamento. Quando ele voltou da fabricação, iniciamos as etapas de medição. Placas de circuito impresso foram desenvolvidas para alimentar, controlar e medir o circuito integrado. As funcionalidades isoladas do circuito foram medidas primeiramente. Após verificarmos que estas estavam de acordo com as expectativas teóricas e de simulação, partimos para o desenvolvimento de um setup completo de medição de umidade relativa. Este setup contém o condicionador de sinais, que é o circuito integrado projetado, uma placa USRP de rádio definido por software, e dois dispositivos SAW-DL, um que atua como o sensor e o outro como a referência. Utilizamos quatro soluções salinas saturadas para criar quatro ambientes com umidades relativas bem controladas e conhecidas. Estas soluções são amplamente utilizadas na calibração de sensores e medidores de umidade. Com este setup realizamos as medições destes quatro ambientes. O controle de temperatura do laboratório durante os testes foi controlado manualmente, e mantido em uma faixa de cerca de 2 ^{o}C.

Resultados e Discussão

O setup de medição de umidade relativa proposto e projetado neste trabalho foi testado em quatro ambientes diferentes com umidade relativa controlada. Os dados obtidos com estas medições demonstram que o sistema responde à umidade relativa mais ou menos como as expectativas teóricas e por simulações. Foi possível medir umidade relativa numa faixa de 32.8 a 90.0 %. Quatro níveis distintos podem ser observados para as quatro condições de umidade. Os resultados foram bem reproduzidos entre dois dias consecutivos. É estimada uma variação de aproximadamente 6 no valor da palavra digital de saída do condicionador para a faixa de umidade relativa testada. Baseado na caracterização do DLL isolado, esta variação na palavra digital de saída se traduz a uma

variação de aproximadamente 15º na fase do sinal elétrico aplicado no sensor SAW-DL.

Considerações finais

Foi possível atingir todos os objetivos propostos para este trabalho. O condicionador proposto foi estudado e posteriormente projetado e testado. Além dos testes isolados, o condicionador foi testado em um setup de medição de umidade relativa. Os resultados experimentais obtidos demonstram a correta operação do condicionador. Apesar de haverem diversas possíveis melhorias no circuito e no setup de medição, os dados obtidos validam a habilidade do sistema para descriminar níveis de umidade relativa.

Palavras-chave: Sensor SAW, malha de travamento de atraso, umidade relativa, CMOS.

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LIST OF ACRONYMS AND SYMBOLS

7BAC - 7-bits accumulator
CMOS - Complementary metal oxide semiconductor
CWA - Chemical warfare agent
DB - Diode bridge
DCDL - Digital-controlled delay line
DLL - Delay-locked loop
DLS - Down level shifter
ESD - Electrostatic discharge
FDIV - Frequency divider
GF - Global Foundries
IC - Integrated circuit
IC2 - Inverter chain buffer of 2 levels
ICBF - Inverter chain buffer
ICMP - Input comparator
IDT - Interdigital transducer
GO - Graphene Oxide
IO - Input/Output
LF - Loop filter
MIM - Metal-insulator-metal
MOS - Metal-oxide-semiconductor
MOSFET - MOS field effect transistor
MOSIS - Metal oxide semiconductor implementation service
NMOS - N-channel MOSFET
OB - Output buffer
P2S - Parallel-to-serial converter
PD - Phase detector
PMOS - P-channel MOSFET
PVA - Polyvinyl alcohol
RH - Relative humidity
SA - Spectrum analyzer
SAW - Surface acoustic wave
SAW-DL - SAW delay-line
SAW-R - SAW resonator
SSS - Saturated saline solution
TB1 - Test board 1
TB2 - Test board 2
TMUX - Test multiplexer

ULS - Up level shifter
VCO - Voltage-controlled oscillator
VCDL - Voltage-controlled delay line
VNA - Vector network analyzer
d - Period of the IDT
K - Frequency division ratio
P_{clk} - Clock period (5 MHz)
P_{ref} - Reference period (160 MHz)
n - Sample number
δ_l - Delay of the “low” delay path
δ_h - Delay of the “high” delay path
δ - Delay difference between δ_h and δ_l
τ_Δ - Total delay caused by the DCDL
τ_{Δ_N} - Delay caused by the Nth delay block
ϕ - Phase difference between signals ddl and sch
τ_s - Delay between signals ref and sch
τ_d - Dealy between signals ref and ddl
τ_r - Delay caused by the reference channel
$\phi_initial$ - Initial phase between signals ddl and sch
R_{DB} - Diode bridge resistor
C_{si} - Internal supply capacitor
Δ_{t_r} - Time-delay between the rising edges of the input and output signals in a delay element
Δ_{t_f} - Time-delay between the falling edges of the input and output signals in a delay element
ϕ_{sr} - Phase between signals sch and rch
R_P - Pull-down resistor
R_C - Resistor used to smooth clock transitions
C_S - Supply capacitor
C_B - Bypass capacitor

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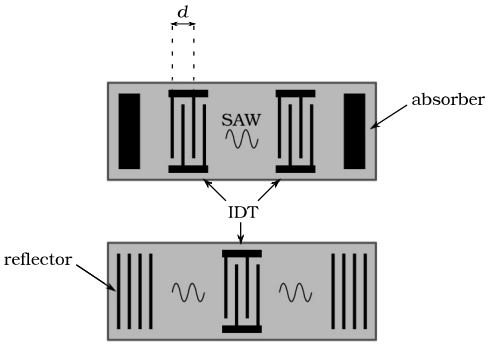
1 INTRODUCTION

Surface Acoustic Wave (SAW) sensors have been demonstrated feasible in a wide variety of applications, acting as transducers of physical, chemical, and biological quantities to electrical quantities. However, the conditioner circuitries generally employed require expensive and large measurement equipments, such as vector network analyzers (VNA), spectrum analyzers (SA), or frequency counters. In this work we propose a novel conditioner for SAW-DL sensors that circumvents the use of these equipments. We also present the design and test of an integrated circuit prototype of this conditioner.

1.1 SAW DEVICES

Surface Acoustic Wave (SAW) devices are electromechanical structures composed of a piezoelectric substrate and at least one electromechanical transducer. Figure 1 shows the two most common forms of these structures, the SAW Delay Line (SAW-DL), and the SAW Resonator (SAW-R). These devices are used in various applications, for instance in the generation of reference signals because of their high frequency stability. They are also often employed in the filtering of signals thanks to their narrow band-pass transfer function. Finally, since the 70s these devices have been used as sensors in a very broad range of applications, such as the sensing of chemical vapors (WOHLTJEN, 1984), temperature (MAINES *et al.*, 1969), humidity (CALIENDO *et al.*, 1997), and more recently the detection of cancer cells and other

Figure 1: Upper view of the two most common SAW devices, the delay line (above) and the resonator (below).



biological structures (CAI *et al.*, 2015).

A piezoelectric solid is a type of material capable of converting an electric field into a mechanical stress (CADY, 1947). Its particular atomic structure creates an electric field in the region where it is mechanically deformed. The inverse effect is also observed: when we apply an electric field the solid deforms. Piezoelectric materials are employed as the SAW devices substrates because of this conversion property aforementioned. Some examples of piezoelectric materials are the quartz, lithium niobate, potassium sodium tartrate (Rochelle salt), barium titanate, etc.

The transduction from an electric signal to a SAW happens by means of the interdigital transducers (IDT) (WHITE; VOLTMER, 1965). These electrodes are formed by the deposition of a thin-layer of metal over the piezoelectric substrate of the SAW device. When a voltage is applied across the terminals of the IDT, an electric field emerges between the fingers. As a consequence, a mechanical deformation occurs at the surface of the substrate, due to its piezoelectric property. If the applied voltage is a periodic signal, a mechanical wave is generated on the surface of the solid. The maximum conversion of energy, from electrical to mechanical, occurs when the wavelength of the SAW equals the period d of the IDT (JR. *et al.*, 1997).

The mechanical wave that is generated in the solid by the process described above is known as a Rayleigh wave, in honor of Lord Rayleigh, pioneer physicist in the studies of waves in solid surfaces (RAYLEIGH, 1885). The particles that compose the surface layers of the solid have two components of displacement, a longitudinal component, i.e., in the direction of the propagating wave, and a component in the direction of the vector normal to the surface (WOHLTJEN, 1984). These two components vibrate, which results in the propagation of a mechanical wave, without the transport of matter. The great majority of the energy associated with this perturbation is within one wavelength depth, and that is why they are called surface waves. This particular characteristic is responsible for the usually high sensitivity of the SAW sensors.

The most common SAW device structures are the delay line (SAW-DL) and the resonator (SAW-R), shown in Figure 1. The SAW-DL is composed of two IDTs and energy absorbers. One of the transducers is used as the transmitter and the other as the receiver of the SAW propagating through the substrate. The absorbers attenuate undesired reflections from the boundaries of the device, thereby ensuring that the flow of energy happens mostly from one transducer to the other. One interesting characteristic is that the delay caused by the SAW-DL is about 10^5 times larger than that caused by an elec-

tric transmission line with the same length (the speed of the Rayleigh wave in a quartz crystal is approximately 3100 m/s, about 10^{-5} times the speed of light in vacuum). This can be used to fabricate much shorter delay lines.

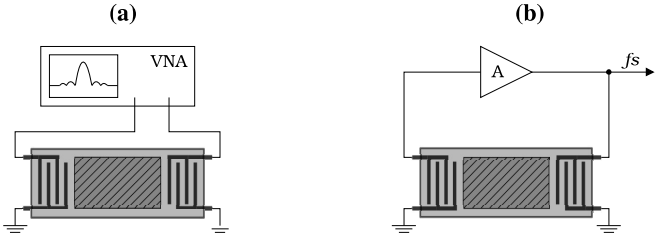
The SAW-R is composed of one IDT and energy reflectors. The transducer serves as both transmitter and receiver of the SAW. The wave that is generated by the IDT propagates through the substrate in both directions, and is reflected back to the IDT with a different amplitude and phase. This difference can be detected by measuring the impedance or reflection coefficient seeing across the IDT terminals. In the resonance frequency, the device presents a complex impedance which is a function of the SAW speed, and the distance between the IDT and the reflectors. These devices are usually employed in oscillator, due to their high frequency stability.

1.2 THE SAW SENSOR

SAW devices can be used as transducers of physical, chemical, and biological quantities to an electric signal. The measurand interacts with the surface on which the SAW is traveling, and this interaction causes a variation in the phase-velocity and amplitude of the propagating wave. This variation can be detected as a shift in the amplitude or delay of the electric signal applied to the sensor. For instances, one can take advantage of the temperature-delay coefficient of a SAW in an specific substrate in order to create a temperature sensor. A form of using SAW devices to sense chemical or biological quantities is to coat the delay-path (surface region through where the SAW propagates) with a material that absorbs or creates bond with the measurand. For instance, the relative humidity sensor used in this work is coated with a thin-layer of graphene oxide (GO), which can absorb water molecules. This causes a mass-loading effect in the surface, which decreases the SAW phase-velocity and increases the propagation delay. In this section we review the most common methods of conditioning SAW sensors, and present some interesting applications and researches.

The most traditional methods of conditioning and measuring a SAW sensor response are presented in Figures 2a and 2b. One can directly measure the frequency response of the device in a VNA and estimate the group delay through the transmission coefficient of the SAW-DL. In the case of a SAW-R, the VNA measures variations in the reflection coefficient as a function of the measurand. This method can offer a high measurement precision, however it requires an expensive and large electronic equipment. Another

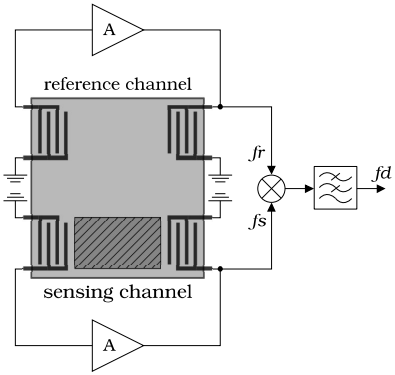
Figure 2: Most common methods of conditioning SAW-DL sensors.



method, which is depicted in Figure 2b, consists of using the SAW device as the element that determines the frequency of an oscillator (MAINES *et al.*, 1969) (WOHLTJEN, 1984). In order for the circuit to oscillate, the Barkhausen criteria must be fulfilled. Therefore, the amplifier A must be able to add enough power to compensate for the insertion loss of the SAW-DL, and the total phase in the loop must be a multiple of 2π. The measurand interacts with the surface and changes the delay of the SAW, which reflects in small variations around the central oscillation frequency, determined by the IDT structure. Therefore, the quantity of the measurand is translated to a variation in the frequency *fs*. Similarly, an oscillator can be made with a SAW-R. Finally, *fs* is measured with a frequency counter, or with a SA. This is by far the most common conditioner for SAW sensors, because it generally offers a high measurement precision. However, it also depends on usually expensive electronic equipments.

An interesting variation of the conditioner presented in Figure 2b was proposed in (REEDER *et al.*, 1975) for compensating temperature in pressure measurements. An adaptation of this architecture is depicted in Figure 3. Two SAW-DL are fabricated over the same substrate. One of them is coated with a thin-film of a sensitive material (sensing channel), and the other is left uncoated (reference channel). The frequency difference *fd* between the reference and sense signals is obtained by mixing and low-pass filtering fr and fs. This new signal contains in its frequency the quantity of the measurand. Since both delay-paths are subjected to the same temperature, because they are in the same substrate and close to each other, both frequencies *fr* and *fs* vary the same amount as a function of this environment parameter. Therefore, temperature variations do not considerably change the frequency *fd*, i.e., this architecture compensates temperature. It can also compensate for aging, since both SAW-DL are subjected to the same environment over time. Although the output signal has a much lower frequency than *fs*, this

Figure 3: SAW-DL sensor conditioner with temperature compensation.



conditioner still requires a form of measuring frequency.

Temperature was the first parameter to be measured with a SAW device (MAINES *et al.*, 1969). The initial intention of the authors was to determine the relation between temperature and delay in order to compensate this undesired behavior in other applications of SAW devices (e.g., transversal filter and dispersive delay line). This research led to a whole new field of study where SAW devices are employed as sensor in a great variety of applications. In temperature SAW sensors, the expansion (or contraction) of the delay-path and changes in the velocity of the mechanical wave due to temperature are used as the transduction mechanism. For instance, the authors in (BORRERO *et al.*, 2013) used a 128° YX cut of $LiNbO_3$ (lithium niobate) to fabricate a SAW-R temperature sensor. The reflection coefficient was measured in a VNA in order to detect the frequency variation in the resonance as a function of the temperature variation. The result was a linear relationship (-5.83 kHz/^{o}C) between the resonance frequency and the temperature.

In chemical and biological SAW sensors a sensitive thin-layer is chosen in order to absorb or to form chemical bonds with a specific analyte or organism. This trapping causes a mass-loading in the surface of the device, which is responsible for the shift in the propagation velocity of the SAW. In (RAJ *et al.*, 2013) four one-port SAW-R devices were covered with four different oxide thin-layers (ZnO, TeO_2, SnO_2, and TiO_2). They were used to compose an E-nose (electronic nose) array to detect chemical warfare agents (CWA), which are vapors very dangerous to humans, even in low concentration. In order to condition the sensors signals, the authors use a circuitry similar to the one presented in Figure 3, where one uncoated device is used

in a reference oscillator, and the other four coated devices are used in four sense oscillators (RAPP *et al.*, 2000). The information is in the frequency difference between the reference and the sense oscillators. In this case a multiplexing technique has to be used in order to allow only one sense oscillator to operate each time. The E-nose array could rightfully classify four CWA simulants (DMMP, DBS, CEPS, and DECP), even in the presence of some interferent vapors (petrol, diesel, kerosene, VOCs, and water).

A great variety of organic and inorganic chemical vapors can be detected by SAW sensors. A few examples are: toluene, octane, methanol, ethanol, alcohol, esters, carboxylic acids, NH_3, CO, CH_4, H_2, O_2, etc. Two vast reviews on SAW vapor sensors are presented in (AFZAL *et al.*, 2013) and (BO *et al.*, 2016).

SAW sensors have also a promising future in biological analysis. In (CAI *et al.*, 2015) a SAW-R operating at 6.4 GHz (third-order harmonic) is used to detect specific mouse cancer cells and DNA bases. The SAW-R is analyzed in a VNA in order to detect frequency shifts in the reflection coefficient as a response to variations in the concentration of these substances. An ultra-high sensitivity was obtained, which makes the sensor able to detect a single hybridized DNA base, and sense two mouse living cancer cells: mammary adenocarcinoma (EMT6) and fibroblast (3T3) cells.

Finally, SAW sensors have been employed in the measurement of humidity levels with relatively high responsivity and small response time (RITTERSMA, 2002), as compared to other humidity sensors (e.g., capacitive and resistive). In (PENZA; CASSANO, 2000) a commercial SAW-DL operating at 433.92 MHz is coated with a PVA (polyvinyl-alcohol) film, a hygroscopic polymer which absorbs water molecules. The absorption causes a mass-loading in the surface of the device, which decreases the propagation velocity of the SAW. The conditioner used in this work is similar to the one presented in Figure 3. In (CALIENDO *et al.*, 1997) the authors investigate the response of several chemical interactive material membranes to relative humidity (RH) on the exposure to water, ethanol, and acetone vapors. They report a considerable variation in the phase velocity and in the acoustic attenuation of the signals propagating along the surface of the SAW-DL as a function of the gas concentration.

In the literature, SAW sensors are widely reported with high sensitivity, fast response time, small size, and reasonable cost (AFZAL *et al.*, 2013), (BO *et al.*, 2016), (LEE; LEE, 2005), (RAPP *et al.*, 2000). The researches presented in this section also demonstrate the wide variety of applications for these sensors, ranging from the transduction of temperature and humi-

Table 1: Selected research on SAW sensors.

	(PENZA; CASSANO, 2000)	(BORRERO *et al.*, 2013)	(RAJ *et al.*, 2013)	(CAI *et al.*, 2015)
Type of SAW sensor	Delay Line	Resonator	Resonator	Resonator
Operating Frequency	468 MHz	65 MHz	433.9 MHz	6.4 GHz (3rd harm)
Measurand	Relative Humidity	Pressure, Temperature, Impedance	Chemical Warfare Agents	Mouse cancer cells and DNA bases
Output Format	Frequency	Reflection Coefficient	Frequency	Reflection Coefficient
Required Equipments	Frequency Counter + PC	VNA	SA	VNA

dity, to the detection of chemical warfare agents and cancer cells. Therefore, the SAW technology has a promising future in sensor applications. Table 1 summarizes the selected researches on SAW sensors presented in this section.

However, the circuitry generally employed in the conditioning of these sensors does not offer a complete solution, as can be notice by the equipments usually required to condition these sensors. As stated in (LEE; LEE, 2005) "In general, gravimetric humidity sensors[1] provide a high sensitivity, a rapid response time and a simple experimental setup. However, they generally require expensive driving and detection electronics". In (BO *et al.*, 2016) it is stated that "Though quite a lot of advantages have been shown for SAW sensors, various challenges still exist. The biggest one is the peripheral circuit. Frequency response and time delay is measured using a network analyzer, which is large and expensive".

1.3 SCOPE OF THIS PROJECT

The references presented in the last section show how vast is the field of SAW sensors. A multitude of physical, chemical, and biological quantities can be translated to variations in amplitude, phase, and/or frequency of an electric signal through these transducers. However, the conditioning of these sensors still relies on large and expensive laboratory equipments (SA, VNA, frequency counter). The main focus of researches is on new sensitive thin-layers to detect different analytes, always relying on the traditional conditioning techniques. Therefore, it is clear that the electronic circuitry which is used to condition the SAW sensors can still be improved. This research

[1] SAW sensors are classified as gravimetric sensors.

focus on the conditioner circuitry for SAW-DL sensors.

The general objective of this work was to design an integrated circuit conditioner for a SAW-DL humidity sensor fabricated by Dr. Sergey Balashov (CTI Renato Archer). The novel conditioner proposed in this dissertation has the main advantage of direct converting the measurand to a digital word, which can be acquired and processed by a microcontroller or computer. Although the focus was to develop a conditioner for the humidity sensor, we understand that the proposed architecture can be extended to any SAW-DL sensor which can translate a measurand of interest to a time-delay of a signal.

The specific objectives of this work were:

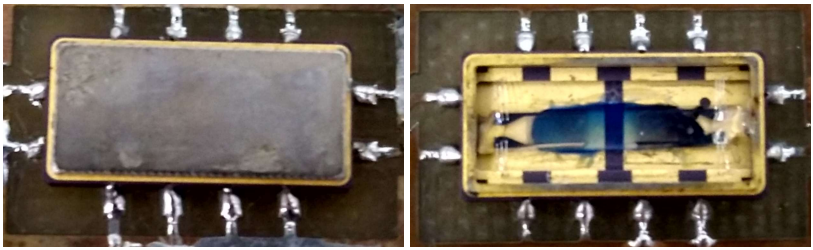
- To study the DLL as a time-delay measurement system, and how it can be applied as the conditioner for SAW-DL sensors;
- To study the proposed architecture through literature review and mathematical models;
- To design an integrated circuit, with special attention to the testability of this circuit;
- To measure the IC stand-alone functionalities;
- To design a reliable setup to measure humidity, containing the sensor and the IC;
- To measure humidity with this setup in order to verify the expected behavior of the proposed conditioner.

1.3.1 Case study - SAW-DL humidity sensor

The SAW-DLs used in this work are depicted in Figures 4a (used as the reference channel) and 4b (used as the sensing channel). They were fabricated on a ST-cut Quartz substrate and coated with a sub-micron-thick film of graphene oxide (GO), which is hygroscopic. The details of the fabrication process of these devices are published elsewhere (BALASHOV *et al.*, 2012). The devices were not especifically designed for this system. These SAW sensors were already fabricated, and we designed the integrated circuit to condition them. Their operating frequency is 160 MHz.

Figure 4: SAW-DL used in this work.

(a) Reference **(b) Sensor**



1.4 NOTATION

The following notation is adopted throughout this document:

- Signals are labeled in lower, italic case. E.g. *up*.
- The inputs and outputs of internal blocks are labeled in lower, bold case. E.g. **up**. Notice that *up* is referring to a signal, and **up** to an IO.
- The inputs and outputs of the integrated circuit and test board pins are labeled in upper, bold case. E.g. **EXTCLK**.
- A signal array is denoted as a[3:0], from MSB to LSB. Similarly, an internal IO array is denoted as **a**[3:0], and an IC IO array as **A[3:0]**.
- In some parts of the analysis, the decimal value of a digital word is required. This is denoted by $\overline{a}$, and should be read as the value of the word *a[3:0]*.
- Blocks, subsystems, and circuit elements are labeled in simple upper case.

2 PROPOSED CONDITIONER FOR SAW-DL SENSORS

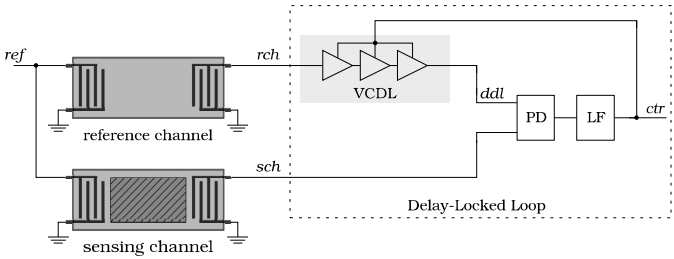
In this chapter we present the proposed signal conditioner for generic SAW-DL sensors (ROTTAVA *et al.*, 2016). The proposed architecture is depicted in Figure 5. It is composed of two SAW-DL devices, one acting as the sensing channel, and one as the reference channel, and a Delay-Locked Loop (DLL). In this architecture the SAW-DL sensor is in open-loop configuration, differing from the most common approach where it is in the feedback loop of an oscillator (see Figure 2b). Therefore, the information about the environmental parameter under measure in conveyed in the delay of a signal, rather than in its frequency. The DLL performs the function of tracking this delay, and by doing so the control signal *ctr* (filtered-error signal) allows a direct measure of the delay.

The chapter starts with a detailed explanation of the novel architecture. Then, we present the fully-digital DLL and analyze it as a discrete-time system. This analysis gives us some important insights about the system behavior.

2.1 DLL-BASED CONDITIONER FOR SAW-DL SENSORS

The proposed conditioner is depicted in Figure 5. A reference signal *ref* is applied to two SAW-DLs, one of them sensitive to an environmental parameter of interest (relative humidity in our case), and the other non-sensitive. The former acts as the sensing channel (whose output is *sch*), and the later as the reference channel (*rch*). Since both devices are in an open-loop configuration, the information we want to measure is conveyed in the time-delay between the signals *sch* and *rch*. This is the fundamental difference between

Figure 5: Diagram of principles of the proposed conditioner.



our measurement setup and the classical one presented in Figure 2b. This time-delay is then measured with a Delay-Locked Loop.

The DLL was first proposed as a form of measuring the time-delay between two correlated signals for radar applications (SPILKER; MAGILL, 1961)[1]. A typical DLL, as the one in Figure 5, is composed of a voltage-controlled delay line (VCDL), a phase detector (PD), and a loop filter (LF). The VCDL is a system that adds delay to the signal *ddl* (in relation to *rch*) in proportion to the voltage level of *ctr*. The PD generates a response proportional to the phase difference between its input signals. The LF is a first-order integrator which accumulates the phase difference throughout the operation in order to generate the control signal *ctr*.

The DLL is a negative-feedback system which controls the VCDL in order to phase-align *ddl* and *sch*. These signals are compared in the PD and the result is integrated in the LF. The filtered-error signal *ctr* is fed back to the VCDL and controls the increment or decrement of the delay between *ddl* and *rch*, in order to phase-align *ddl* to *sch*. Once the system reaches equilibrium, the time-delay between the signals in the input of the PD is kept constant throughout operation, as long as perturbations are not too strong, and the blocks do not saturate.

Perturbations in the time-delay of the input signals *sch* and *rch* are compensated by the system in the direction of phase-aligning *ddl* and *sch*. For instance, if the environmental parameter to be measured acts in the sensing channel by increasing the delay of *sch* in relation to *rch*, the delay caused by the VCDL also has to increase in the same amount in order to maintain the system locked in delay. Once the DLL reaches the new equilibrium, the value of the filtered-error signal *ctr* is increased in proportion to the increment in the delay of the sensing channel. Therefore, the proposed architecture directly converts variations in the environmental parameter being measured by the SAW-DL into a voltage level.

The reference channel serves to compensate for temperature (BALASHOV *et al.*, 2014). If the two devices are fabricated over the same substrate, the temperature will equally affect both delay paths, which will make the delays in signals *rch* and *sch* increase in the same proportion. The result is a desensitization of the system response to temperature. However, in this work we only had access to separate SAW devices for the reference and sensing channels. Therefore, the compensation is not guaranteed, since the

[1] The system is called Delay-Lock Discriminator. The DLL is a more generic system which can be use to measure time-delays (in the case of this publication), but also in data and clock recovery, and a great variety of other applications.

devices are in different substrates and are distant from each other.

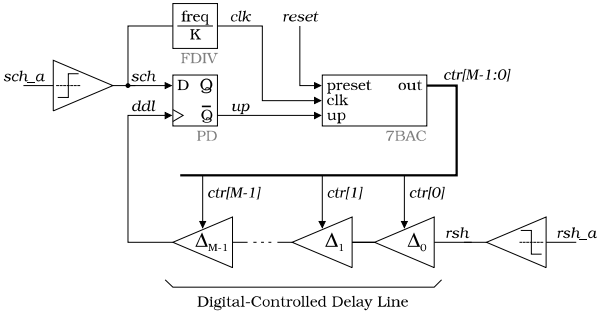
The next section presents the fully-digital implementation of the DLL which was used in this work. Each block of the system is described in detail, and a simplified model for the DLL is developed to demonstrate its principle of operation. For a more detailed analysis of the DLL operation, the reader is referred to (KIM *et al.*, 2003).

2.2 THE FULLY-DIGITAL DLL

Voltage-controlled delay lines are frequently designed with a MOS transistor as a voltage controlled resistor in a RC filter, or with a current starving structure as the element to control the delay (BAE *et al.*, 2005) (KUO; MA, 2013). This results in a non-linear transfer function for this block. Since the behaviour of the SAW-DL sensor was not known previously to the design (its delay vs RH response), we decided to investigate a VCDL with a linear (or at least nearly linear) response. This led us to the idea of creating small delay elements with only two possible states: a "high" delay path and a "low" delay path. These delay elements are concatenated to create what we call a Digital-Controlled Delay Line (DCDL), which is controlled by a digital word, instead of a voltage level. Since our control element is digital, we decided to adopt a fully-digital architecture for the rest of the DLL (MESGARZADEH; ALVANDPOUR, 2009). A fully-digital structure also has the advantages of low-area consumption.

The block diagram for the fully-digital DLL is presented in Figure 6. It is composed of two input comparators, a D flip-flop employed as the PD, a frequency divider (FDIV), an M-bit counter, and the DCDL. The incoming

Figure 6: The fully-digital DLL.



signals from the SAW devices are digitized in the comparators to obtain *rch* and *sch*. Apart from these two blocks, all the remaining blocks can be fully-implemented with standard logic circuits. The rest of this chapter is dedicated to a discussion and analysis of each individual block, followed by a mathematical modeling of the whole system.

2.2.1 Input Comparators

The function of the input comparators is to saturate the incoming signals from the SAW devices to high and low logic levels. The only important information we want from these signals is their transitions (rising and falling edges), which convey their phase. Therefore, the function of the input comparators is to convert the low-amplitude sinusoidal signals into rail-to-rail square signals.

2.2.2 Frequency divider

The state of the system is updated every rising edge of *clk*. This signal is generated by dividing the frequency of *sch* (which is the same of *ref* frequency) by K. Therefore, the *clk* period is given by:

$$P_{clk} = K P_{ref}, \tag{1}$$

where P_{ref} is the period of the reference signal. From now on, in order to model the DLL we will use the variable n to represent the sample number, i.e., one *clk* period.

2.2.3 Phase detector

The phase detection is performed by a D flip-flop. If the rising edge of the signal *ddl*, which is being applied to the clock input of the flip-flop, occurs before the rising edge of *sch*, applied to the D input, it means that the former is phase-advance in relation to the latter. As a result, signal *up* receives logic level '1'. The other possibility is that *ddl* is phase-delayed in relation to *sch*. In this case, *up* goes to logic level '0'.

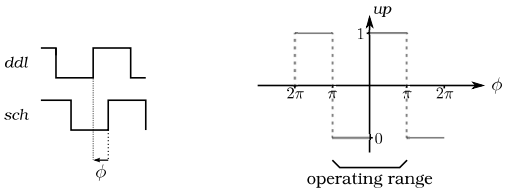
The phase difference between signals *ddl* and *sch* as a function of the

delays from *ref* to *ddl* (τ_d) and from *ref* to *sch* (τ_s) is given by:

$$\phi[n] = \frac{2\pi}{P_{ref}} \left(\tau_s[n] - \tau_d[n] \right), \tag{2}$$

where the term $2\pi/P_{ref}$ converts a time-delay into a phase-delay. This PD can only detect the wrapped phase difference in the range $(-\pi, \pi)$ between the two signals, as illustrated in Figure 7. Therefore, the result of Equation 2 must be wrapped to the interval $(-\pi, \pi)$.

Figure 7: Phase detector response.



Once the system reaches an equilibrium, the phase difference $\phi[n]$ must never surpass $\pm\pi$, otherwise the system will reach another equilibrium (one reference period before, or one after). In other words, the system must be fast enough in order to compensate any possible perturbation in the delay of the signal *sch* caused by variations in the measurand.

The result generated by the PD as a function of the wrapped phase difference is then:

$$up[n] = \begin{cases} \text{`0'}, & \text{if} \quad -\pi < \phi[n] < 0 \\ \text{`1'}, & \text{if} \quad 0 < \phi[n] < \pi \end{cases} \tag{3}$$

This PD generates only two possible outcomes: signal *ddl* is either phase-advanced in relation to *sch*, which makes *up* = '1', or it is phase-delayed, which makes *up* = '0'. Therefore, the borders of the two signals will never be perfectly aligned. Even when the system reaches equilibrium, and there are no external perturbations, there will always be an oscillation between at least two states of the accumulator. This can be treated as quantization noise which is observed in analog-to-digital conversion.

2.2.4 M-bit counter

The M-bit counter serves as a first-order integrator, or an accumulator. Its rate of update is determined by the signal *clk*. At each rising edge of this signal, the counter accumulates a unit depending on the value of the flag *up*. If $up[n-1]$ = '0', the value of the digital word $ctr[M-1:0]$, namely $\overline{ctr}$, is decreased by 1, else $\overline{ctr}$ is increased by 1. We can model the behavior of the counter at sample n as:

$$\overline{ctr}[n] = \begin{cases} \overline{ctr}[n-1]-1, & \text{if } up[n-1] = \text{`0`} \\ \overline{ctr}[n-1]+1, & \text{if } up[n-1] = \text{`1`} \end{cases} \tag{4}$$

or in terms of the wrapped phase ϕ:

$$\overline{ctr}[n] = \begin{cases} \overline{ctr}[n-1]-1, & \text{if } -\pi < \phi[n-1] < 0 \\ \overline{ctr}[n-1]+1, & \text{if } 0 < \phi[n-1] < \pi \end{cases} \tag{5}$$

Notice that $ctr[N]$ means the N^{th} bit of the digital word, and $\overline{ctr}[n]$ means the decimal value of the digital word at sample n, which is given by:

$$\overline{ctr} = 2^0 ctr[0] + 2^1 ctr[1] + ... + 2^{M-1} ctr[M-1]. \tag{6}$$

The counter can be asynchronously set to a predefined value when *reset* signal is high, which allows us to force an initial state in the system. This value is chosen $2^M/2$, half the maximum value of $\overline{ctr}$, in order to allow the system to swing in both directions, increasing or decreasing the delay of the DCDL.

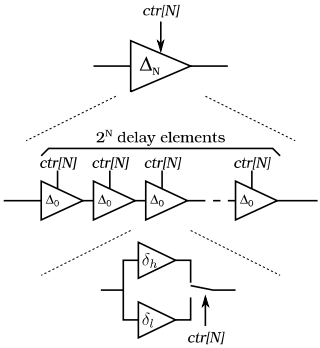
The value of $\overline{ctr}$ is limited to the interval $[0, 2^M - 1]$. When these limits are reached, the controller no longer follows the behavior of Equation 4. These limits must be avoided by the designer.

2.2.5 Digital-Controlled Delay Line

The DCDL is composed of M delay blocks, Δ_0 to Δ_{M-1}. Each delay block is composed of a number of cascaded delay elements, which increases by a power of two at each level. Therefore, the N^{th} delay block has 2^N delay elements, as depicted in Figure 8. A delay element can be realized by a few inverters and a few switches to choose between a "high" delay-path (δ_h seconds of delay) and a "low" delay-path (δ_l seconds of delay). This implemen-

tation circumvents the use of non-linear devices for controlling the delay of the VCDL, avoiding undesired non-linear effects. This is important because the conversion gain of the DLL is directly related to the transfer function of the DCDL.

Figure 8: Nth delay block structure.



The time-delay caused by the Nth delay block is given by:

$$\tau_{\Delta_N} = 2^N \left[\delta ctr[N] + \delta_l\right], \tag{7}$$

where δ = δ_h - δ_l is called the delay step or gain of the DCDL. The total time-delay caused by the DCDL is the summation of the time-delays of each delay block:

$$\tau_\Delta = \tau_{\Delta_0} + \tau_{\Delta_1} + ... + \tau_{\Delta_{M-1}}, \tag{8}$$

which can be written in terms of $\overline{ctr}[n]$ as:

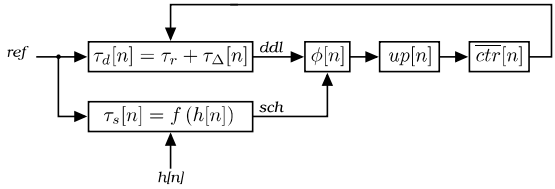
$$\tau_\Delta[n] = \delta\, \overline{ctr}[n] + (2^M - 1)\delta_l. \tag{9}$$

2.2.6 Fully-digital DLL analysis

A model for the fully-digital DLL as a discrete-time system is presented in Figure 9. The mathematical models for each block were obtained based on the behavior we expect for each one. Now we develop a mathematical analysis of this system, which gives us some important insights about its operation.

The time-delay between *ref* and *ddl* at sample n is the sum of the delay caused by the reference SAW-DL τ_r and the delay caused by the DCDL $\tau_\Delta[n]$:

Figure 9: Discrete-time model for the fully-digital DLL.



$$\begin{aligned}\tau_d[n] &= \tau_\Delta[n] + \tau_r \\ &= \delta\,\overline{ctr}[n] + (2^M - 1)\delta_l + \tau_r.\end{aligned} \tag{10}$$

The time-delay between *ref* and *sch* at sample n equals the delay caused by the sensing SAW-DL, which is related to the measurand value $h[n]$:

$$\tau_s[n] = f(h[n]), \tag{11}$$

where $f()$ is the function that relates the measurand to the delay caused by the sensing device.

Equation 2 can be written in terms of an initial wrapped-phase $\phi[0]$ and variations in the delays τ_s and τ_d with respect to an arbitrary initial sample (n = 0) as:

$$\phi[n] = \phi[0] + \frac{2\pi}{P_{ref}}\left[(\tau_s[n] - \tau_s[0]) - (\tau_d[n] - \tau_d[0])\right]. \tag{12}$$

By replacing Equations 10 and 11 into Equation 12 we get:

$$\phi[n] = \phi[0] + \frac{2\pi}{P_{ref}}\left\{\left[f(h[n]) - f(h[0])\right] - \left[\delta\,\overline{ctr}[n] - \delta\,\overline{ctr}[0]\right]\right\}. \tag{13}$$

Let us first analyze this equation when there is no external perturbation, i.e., the measurand $h[n]$ does not change from its initial value $h[0]$. Hence, Equation 13 simplifies to:

$$\begin{aligned}\phi[n] &= -\delta\,\overline{ctr}[n]\frac{2\pi}{P_{ref}} + \phi[0] + \delta\,\overline{ctr}[0]\frac{2\pi}{P_{ref}} \\ &= -\delta\,\overline{ctr}[n]\frac{2\pi}{P_{ref}} + \phi_{\text{initial}}.\end{aligned} \tag{14}$$

For practical reasons the value of δ will always be a small fraction of the

period P_{ref}, since the smaller its value, the higher the conversion gain of the DLL[2]. If ϕ starts negative, the next value of $\overline{ctr}$ will be decreased by 1, which will bring ϕ closer to 0. On the other hand, if ϕ starts positive, the next value of $\overline{ctr}$ will be incremented by 1, also bringing the next value of ϕ closer to 0. Regardless of the value of $\phi_{initial}$, the system will always converge to a state where the phase approaches 0 (as long as $\delta < P_{ref}/2$). As explained before, the PD only generates two outcomes: *ddl* is either phase-advanced or phase-delayed in relation to *sch*. For this reason, after reaching equilibrium the value of ϕ will have an oscillation between a slightly positive and a slightly negative value.

Therefore, when there is no external perturbation ($f(h[n]) = f(h[0])$ for all n), the system will always reach an stable equilibrium, as long as $\delta < P_{ref}/2$, and the M-bit counter does not saturate. The first condition is not a big concern, since we will usually wish the lowest δ possible, and the second condition is achieved by properly designing the DCDL and the M-bit counter. The next important question to answer is: assuming that the delay caused by the sensing SAW-DL increases linearly ($f(h[n]) = \alpha n$), what is the maximum slope α in order for the system to remain locked?

To answer this question we start by rewriting Equation 2 in the form of a difference equation and then replace 10 and 11 into it:

$$\begin{aligned}\phi[n] &= \phi[n-1] \\ &\quad + \frac{2\pi}{P_{ref}} \left\{ [f(h[n]) - f(h[n-1])] - \delta \ [\overline{ctr}[n] - \overline{ctr}[n-1]] \right\}.\end{aligned} \tag{15}$$

The term $f(h[n]) - f(h[n-1])$ reduces to α. Let us assume that α is positive, and big enough so that the value of $\overline{ctr}$ has to be increased at every cycle in order for the system to track this variations in the delay of the sensing SAW-DL. Therefore, $\overline{ctr}[n] - \overline{ctr}[n-1]$ is 1, and Equation 15 simplifies to:

$$\phi[n] - \phi[n-1] = \frac{2\pi}{P_{ref}} (\alpha - \delta). \tag{16}$$

Let us take a look back in Figure 7. The delay in signal *sch* is increasing, which in turn causes an increase in ϕ. However, the system will try to track the delay of *sch* by adding more delay to signal *ddl*. The system is kept locked if the phase ϕ is kept below π. This means that the rate of variation in the

[2] If $\delta > P_{ref}/2$, the system can jump from one stable equilibrium to another or even become unstable, specially when $\delta > P_{ref}$.

delay of *ddl* must be higher than the rate of variation in the delay of *sch*, which translates to a negative variation of ϕ. Therefore:

$$\begin{aligned} \phi[n] - \phi[n-1] &< 0 \\ \frac{2\pi}{P_{ref}}(\alpha - \delta) &< 0, \end{aligned} \tag{17}$$

and the limit to the value of α is:

$$\alpha < \delta \tag{18}$$

An analogous analysis can be made for a negative α, which results in the condition $\alpha > -\delta$.

But what does the value of α actually mean? The expression $f(h[n]) = \alpha n$ translates to $f(h(t)) = (\alpha/P_{clk})t$ in continuous-time. Therefore, the parameter α/P_{clk} is the rate of variation in the delay caused by the sensing SAW-DL, in seconds-per-second. As a consequence of condition 18, the maximum value of this parameter is $|\delta|/P_{clk}$. We can increase it by speeding-up the system, i.e., making P_{clk} smaller. However, variations in the delay caused by the sensing SAW-DL will usually be extremelly slower than the rate of update of our system, and therefore the condition of Equation 18 is met without any speciall effort.

By giving enough time, respecting the conditions for the value of δ and α, and ensuring that the DCDL and the M-bit counter have the necessary tracking range, the system will keep track of the delay caused by the sensing SAW-DL. Since α will usually be much lower than δ, once the system reaches equilibrium the phase ϕ will be kept close to 0. Therefore, we arrive to an expression for $\overline{ctr}[n]$ from Equation 13:

$$\overline{ctr}[n] = \frac{f(h[n])}{\delta} + \frac{P_{ref}}{\delta 2\pi}\phi[0] - \frac{f(h[0])}{\delta} + \overline{ctr}[0]. \tag{19}$$

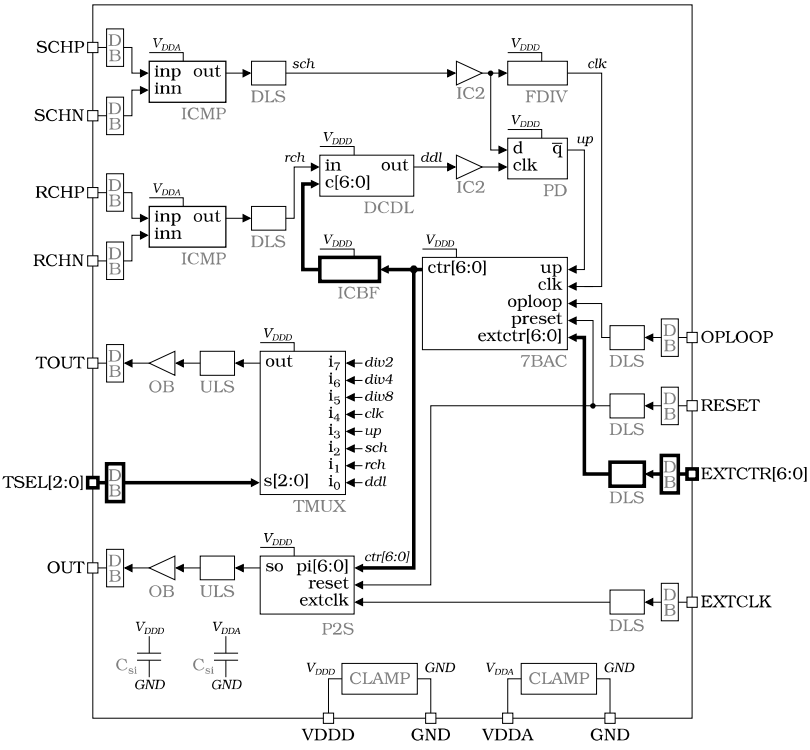
Hence, the value of $\overline{ctr}[n]$ is directly proportional to the delay caused by the sensing SAW-DL ($f(h[n])$), and inversely proportional to the gain of the DCDL (δ).

To conclude, Equation 19 shows that the fully-digital DLL presented in Figure 6, under the right operating ranges, can be used to convert variations in the time-delay of a SAW-DL sensor into a digital word.

3 CMOS CONDITIONER FOR A SAW-DL HUMIDITY SENSOR

This chapter presents the design decisions, topologies, and the most relevant simulation results of each individual block, as well as the integration of the whole system. In order to transform the idea proposed in the last chapter into an actual integrated circuit with the desired functionalities, several decisions were made and restrictions were imposed. This led us to the block diagram of the system presented in Figure 10. This diagram is a complete representation of the fabricated IC.

Figure 10: Block diagram of the designed integrated circuit.



3.1 SYSTEM TOPOLOGY AND TECHNOLOGY

The blocks that compose the system are:

- DB, CLAMP: Diode bridge and power clamp, electrostatic discharge protection circuits;
- ICMP: Input Comparator;
- DLS: Down Level Shifter;
- IC2: Inverter Chain buffer of 2 levels;
- FDIV: Frequency Divider;
- DCDL: Digital-Controlled Delay Line;
- PD: Phase Detector
- ICBF: Inverter Chain Buffers;
- 7BAC: 7-bits Accumulator;
- OB: Output Buffer;
- ULS: Up Level Shifter;
- TMUX: Test Multiplexer;
- P2S: Parallel-to-Serial Converter;
- C_{si}: Internal supply capacitors.

If we compare the DLL struture presented in Figure 6 and its actual implementation presented in Figure 10 we notice an additional block ICBF between the DCDL and the accumulator. Some of the **c[6:0]** inputs of the DCDL contain hundreds of gates, and therefore, the block ICBF serves to strengthen the signal *ctr*[6:0] before appling it to the DCDL. Moreover, this block helps to isolate *ctr*[6:0] from all the noise generated by the DCDL. Besides the buffers, a parallel-to-serial and a test multiplexer were added to the design. The former converts a parallel word of 8 bits into a serial data stream at a rate determined by an external clock signal applied to pin **EXTCLK**. The latter block allows us to measure 8 internal signals for testing and debugging purposes (*div2*, *div4*, and *div8* are P2S internal signals).

The accumulator has two additional inputs: **oploop** and **extctr[6:0]**. The first one alows us to open the DLL loop by forcing the output **ctr[6:0]** of the accumulator to be equal to the external control word applied to **extctr[6:0]**. This function was included for testing purposes. By opening the loop and applying an external control word, we can measure the delay caused by the DCDL for each value of the word. Moreover, we can test whether the P2S is functioning properly or not by applying a known word to **extctr[6:0]**, and observing the output data stream in **OUT**.

The P2S outputs a data stream corresponding to a parallel word of 8 bits (1 byte). However, we chose to design the system with a control word of length 7 (*ctr*[6:0]), and let the last bit to a known level (low level, in this case). This known bit is used as a form of verifying that the parallel-to-serial conversion and the data acquisition are performed correctly. As we shall see in the next chapter, in the script we use to process the signal acquired in the output there is a verification of this last bit. If its value is not low, this is an indication that either the parallel-to-serial conversion or the data acquisition is incorrect.

The *clk* rate must be fast enough in order to track variation in the delay of the sensing channel. On the other hand, the *clk* period must be large enough in order to allow all internal signal to stabilize in the new state before computing the next state. We decided to divide the reference signal of 160 MHz by 32 in the frequency divider in order to meet these requirements.

The system is supplied with two voltage rails: 1.2 V, the core voltage labeled V_{DDD}, and 3.3 V, the IO voltage labeled V_{DDA}. We decided to use two voltage rails to have the internal blocks (the processing parts) built with faster and lower power devices, and the IO blocks built with devices less susceptible to ESD breakdowns[1]. The interface between these two voltage domains is accomplished through the level shifters. The DLS converts a digital signal from the IO voltage rail to the core rail. The ULS makes the opposite conversion. The signals applied to **TSEL[2:0]** were not shifted down. Fortunately, the protections were enough to prevent ESD breakdowns.

This project was designed in technology GF (Global Foundries) CMOS 130 nm, available through the educational program of MOSIS. We used two types of transistors: one for the core blocks, which has a minimum gate length of 120 nm and is supplied with 1.2 V (V_{DDD}), and one for the IO blocks, which has a minimum gate length of 400 nm and is supplied with 3.3 V (V_{DDA}). Both of them are standard devices and do not require any special fabrication step. We also make use of MIM (Metal-Insulator-Metal)

[1] IO devices have a thicker oxide, which makes their breakdown voltage higher.

capacitors between the supply rails and ground in order to reduce the noise injected by the external supply sources. Integrated resistors are used in the ESD protection circuits as well as in the Input Comparators. There are 7 levels of metal available for routing signals and power. The 3 bottom-most metals are used for routing internal signals, and the 4 top-most metals for the power distribution network and for IO signals, except in some special cases.

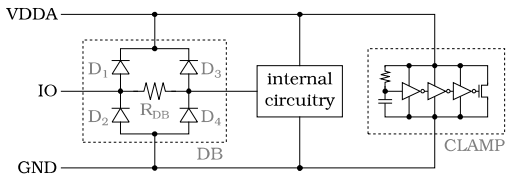
3.2 ESD PROTECTION

The protection against electrostatic discharges (ESD) is of utmost importance in the design of integrated circuits. ESD events may happen during the fabrication and/or handling of the IC, and they can cause temporary or even permanent damages to the devices (GREASON; CASTLE, 1984). MOSFETs are susceptible to ESDs because of their capacitive nature. When a charge is induced in the gate of a MOSFET device, for instance due to contact to a charged human body or machine, a voltage proportional to this charge and inversely proportional to the gate capacitance is induced in the gate of the device. If this voltage is high enough, the dielectric that separates the gate from the bulk breaks, and an electric arc happens due to the high potential difference. This causes damage to the device. Moreover, as the CMOS technology scales down, so does the oxide thickness (t_{ox}), which makes the devices even more susceptible to ESD events. Therefore, in our design we included circuits that provide a path to the induced charges in order to avoid ESD events.

The ESD protection structure used in all the **IO** pins is presented in Figure 11. The aim of using this structure is to prevent that charges induced between an **IO** pin and supply rails reach the gates of the transistors (internal circuitry) and, therefore, avoid ESD events. Under a normal operation of the system, the power clamp is an open circuit. However, when a steep transition in the voltage between **VDDA** and **GND** happens, the power clamp shorts these rails causing a high current leakage between them for a short period of time (controlled by the RC constant of the clamp). The diode bridge (DB) provides a path to the induced charges from the **IO** pin to the supply rails. The flow of currents happens as follow:

- If a charge is induced in such a way that a positive voltage pulse appears in **IO** with respect to **VDDA**, diode D_1 becomes forward biased, and a current flows from **IO** to **VDDA**. This current significantly reduces the amount of induced charges that reach the gates.

Figure 11: ESD protection structure for the IO pins.



- If a charge is induced in such a way that a negative voltage pulse appears in **IO** with respect to **GND**, diode D_2 becomes forward biased, and a current flows from **IO** to **VDDA**. This current also significantly reduces the amount of induced charges that reach the gates.

Therefore, the diode bridge together with the power clamp provide a path to charges induced between the IO and the supply pins.

The resistor R_{DB} provides a path with higher impedance to the induced charges, in order to force them to flow through D_1, D_2, and the power clamp. There is a second path through D_3 and D_4 for the charges that cross R_{DB}, in order to increase the ESD protection of the internal circuitry. The higher the value of R_{DB}, the better the protection. However, this resistance influences the performance of the system, since it attenuates the signals flowing in and out of the IC. We set this resistance to 1.1 kΩ. When measuring the outputs of the system, we will use a voltage probe with 15 pF of capacitance. This ESD protection resistance and the voltage probe capacitance create a low-pass filter with a cut-off frequency of 9.6 MHz, around two times higher than the maximum frequency we wish to measure (5 MHz, the internal clock signal). Therefore, the ESD structure will not prevent the correct measurement of the output signals, though it will attenuate its harmonics. On the other hand, the input signals that come from the SAW-DL have a frequency of 160 MHz. Thus, the ESD structure has to be considered in the design and simulation of the input comparators.

3.3 DIGITAL LIBRARY

Except for the input comparators and the level shifters, the system is entirely composed of standard logic gates and registers. Therefore, the first part in the design was to create a digital library with the schematic and layout views of all the digital circuits necessary for the other blocks. These circuits are all supplied with the core voltage V_{DDD} = 1.2 V, except for the IO inverters,

which are supplied with V_{DDA} = 3.3 V.

3.3.1 Combinational Logic

The design criteria for the core inverter, which uses 1v2 devices, were:

- Minimum gate length: to reduce power consumption, and the propagation delay;

- Threshold in the mid-point between V_{DDD} and GND: to ensure equal high and low noise margins, and to have an output signal with the same duty-cycle as the input signal [2].

These two criteria are not sufficient to determine all the inverter parameters. An additional layout criterion was used: the minimum W for the NMOS in order to have two contacts to the active regions of this device [3]. Hence, the W/L for the NMOS is set to 680nm/120nm, and for the PMOS is set to 2μm/120nm. The NAND and NOR gates (both with 2 and 3 inputs) were designed with the same transistor dimensions as the inverter. Figure 56 in Appendix C shows the layouts of the inverter, a 2 inputs NAND, and a 2 inputs NOR.

The design criteria for the IO inverter were the same as for the core inverter, but using 3v3 devices. The W/L for the NMOS is set to 2μm/400nm and for the PMOS is set to 4μm/400nm. The layout of this circuit is similar to the core inverter, presented in Figure 56a.

3.3.2 D Flip-Flop

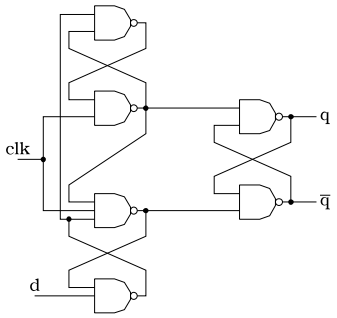
The D flip-flop is employed in many blocks of the system. Two versions of this circuit were required: one with the functions preset and reset, and one without these functions. The topologies for the two versions are presented in Figure 12 (MANO; CILETTI, 2006). The layout of the D flip-flop with asynchronous preset and reset is presented in Figure 57 of Appendix C.

[2] This is important because in the DCDL hundreds of inverters will be cascaded.

[3] A better criterion for a future prototype would be an optimization to reduce the propagation delay, which would in turn reduce the value of δ, and therefore increase the system responsivity.

Figure 12: D flip-flop topologies.

(a) Without preset and reset.



(b) With preset and reset.

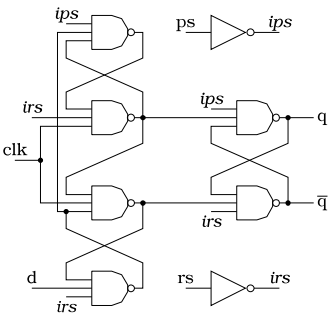
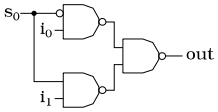
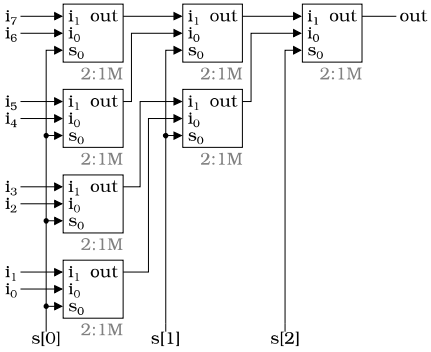


Figure 13: Multiplexer topology.

(a) 2:1M.



(b) 8:1M.

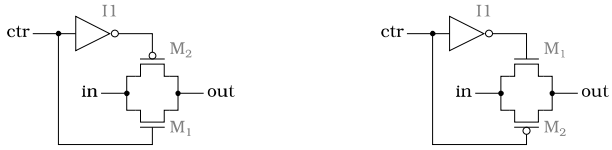


3.3.3 Multiplexers

The system requires two types of multiplexers: a 2:1 (two inputs, one output) and an 8:1. The standard topology of a 2:1M used in this project is depicted in Figure 13a. An 8:1M can be obtained with seven 2:1M, as presented in Figure 13b. The layout of the 8:1M is depicted in Figure 58 of Appendix C.

Figure 14: Three-state switches topology.

(a) Non-inverted control **(b) Inverted control**



3.3.4 Three-State Switches

Three-state switches are used in the DCDL in order to choose between two delay-paths (see Figure 23). These switches are implemented as shows Figure 14. The first one (14a) opens the output node when the signal applied to **ctr** is low, and transmits the signal applied to **in** when the signal in **ctr** is high. The second (14b) realizes the oposite function, transmitting when **ctr** is low, and opening the output when **ctr** is high. The dimensions of transistors M_1 are 680nm/120nm, and M_2 are 1.5μm/120nm. The layout of the three-state switch with non-inverted control is presented in Figure 59 in Appendix C.

3.4 LEVEL SHIFTERS

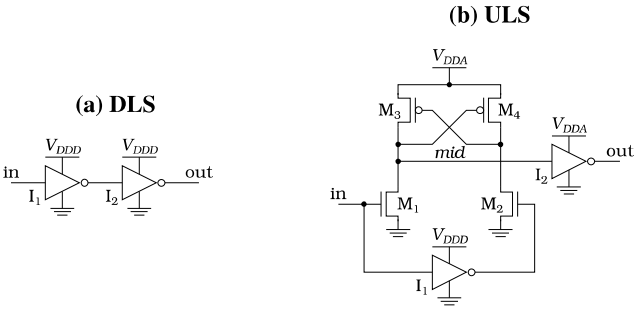
The function of the level shifters is to convert a digital signal from one voltage rail to the other. The up level shifter (ULS) gets a digital signal in the core voltage rail and converts it to the IO voltage rail. The down level shifter (DLS) converts from core to IO voltage rail.

3.4.1 Topology

The topologies of the DLS and ULS are presented in Figures 15a and 15b, respectively. The DLS is composed of two cascaded IO inverters supplied with the core voltage. We use IO inverters because the signal applied to the input of the DLS is in the IO voltage rail.

The ULS is supplied with the two voltage rails, and it is composed of a cross-coupled amplifier (M_1, M_2, M_3, and M_4), a core inverter (I_1), and an IO inverter (I_2). The cross-coupled structure adds a positive-feedback to

Figure 15: Level shifters topologies.



the amplifier, which makes the internal node *mid* to saturate in either V_{DDA} or *GND*. This topology of ULS avoids current leakages, except in the transitions, because either M_1 and M_4 or M_2 and M_3 will be in the cut-off region. The dimensions of transistors M_1 and M_2 are 8μm/400nm, and of transistors M_3 and M_4 are 3μm/400nm. They are all 3v3 devices, since they are supplied with the IO voltage rail. The layouts of the DLS and ULS are presented in Figures 60a and 60b in Appendix C.

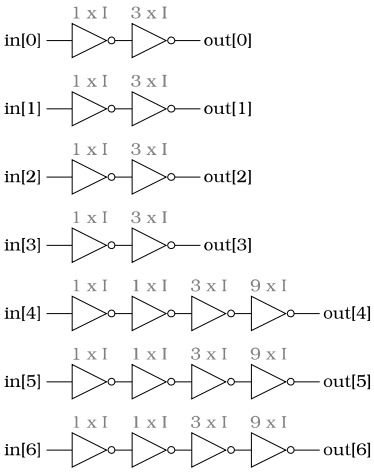
3.5 INVERTER CHAIN BUFFERS

The ICBF block is supplied with the core voltage V_{DDD} and has seven digital inputs and seven digital outputs. The function of this block is to drive the DCDL inputs **c[6:0]** with the control word *ctr*[6:0] generated in the accumulator. The ICBF is used to avoid fan-out issues that could have happened if the 7BAC outputs were connected directly to the DCDL inputs. This block also serves to better isolate the noise generated by the DCDL, where hundreds of inverters are switching within one reference period, from the control word, which is the information sent to the output.

3.5.1 Topology

The ICBF is composed of seven inverter chains, as depicted in Figure 16. The "I" stands for one standard core inverter. The IC2 and the OB blocks are also inverter chain buffers. The former is equal to the top branch in Figure 16, i.e., two inverters, and the latter is equal to the bottom branch, i.e., four

Figure 16: Inverter chain buffers topology.



inverters. The layouts of these buffers are depicted in Figure 61.

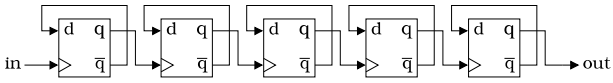
3.6 FREQUENCY DIVIDER

The frequency divider is supplied with the core voltage V_{DDD} and has one input and one output at the same voltage rail. The digital signal at the output has a frequency 32 times smaller than the frequency of the input signal.

3.6.1 Topology

The topology of the frequency divider is presented in Figure 17. Each stage, which is a D flip-flop with its inverted output connected to its **d** input, divides the frequency of the signal applied to the clock input by 2. By dividing the input signal frequency by 2 for five times sequentially, the result is a division by 32. The layout of this block is depicted in Figure 62 in Appendix C.

Figure 17: Frequency divider.



3.7 7-BITS ACCUMULATOR

The 7BAC is supplied with the core voltage V_{DDD} and has five inputs and one output at the same voltage rail. The inputs are:

- **clk**: The signal applied to this input comes from the frequency divider and paces the counter update. This signal has a frequency of 5 MHz.
- **up**: This input controls whether the counter should increase or decrease the value of its state by 1. If the signal applied to this pin is low the next value is decreased by 1, else it is increase by 1.
- **preset**: When this input is high, the decimal value of **ctr[6:0]** is asynchronously set to its mid-value, i.e., 64 (or in binary 1 0 0 0 0 0 0).
- **oploop**: When this input is high, the accumulator output is switched from the counter output to an external control word applied to **extctr[6:0]**, regardless of the signals applied to **clk**, **up**, and **preset**.
- **extctr[6:0]**: An external 7-bits word that sets up the state of the accumulator when **oploop** is high.

The output is:

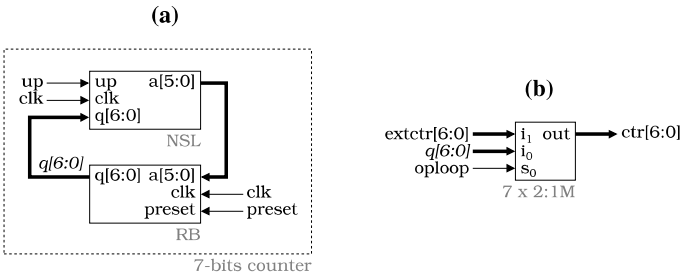
- **ctr[6:0]**: A 7-bits word that represents the state of the accumulator and controls the DCDL.

3.7.1 Topology

Figure 18 presents the topology of the 7-bits accumulator. It is composed of a 7-bits counter (Register Bank and Next State Logic) and 7 2:1 multiplexers. These multiplexers are used to switch the accumulator output **ctr[6:0]** between the counter output q[6:0] and the external word applied to **extctr[6:0]**. When **preset** is low, the 7-bits counter has to implement the following function: at each rising edge of **clk**, $\overline{ctr}$ has to be increased by one if *up* is high, or decreased by one if **up** is low. Therefore, we can sum up the behavior of the counter as follows[4]:

[4] index $_n$ denotes the next value of the bit, and index $_p$ denotes the present value of the bit.

Figure 18: 7-bits accumulator topology.



- $q_n[0] = \overline{q}_p[0]$ regardless of the value of **up**, since if we increase or decrease a number by 1 the LSB of its binary representation will always change its value;

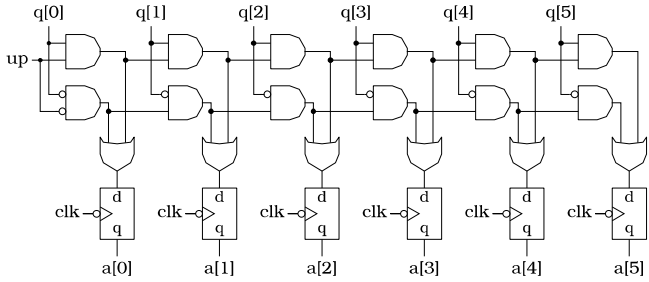
- $q_n[N] = \overline{q}_p[N]$ if all precedent ($q_p[N-1]$ to $q_p[0]$) bits are high and **up** is high, or if all precedent bits are low and **up** is low. Else $q_n[N] = q_p[N]$.

For instance, if the present q word is (from MSB to LSB) 1 0 0 1 1 1 1 and **up** is high the first (LSB) bit will invert since it always inverts, and the second to the fifth will also invert since in all cases the precedents are high and **up** is high. The sixth and the seventh will not invert since at least one of their precedents is low. Therefore, the next word is 1 0 1 0 0 0 0. Another example, if the present word is 0 1 0 1 0 0 0 and **up** is low the first to the fourth bits will invert and the rest will not, resulting in a next word 0 1 0 0 1 1 1. Following this logic, in the special case when the present word is 1 1 1 1 1 1 1 and **up** is high, the next word is 0 0 0 0 0 0 0. Similarly, when the present word is 0 0 0 0 0 0 0 and **up** is low, the next word is 1 1 1 1 1 1 1.

The circuit that implements the next state logic (NSL) is depicted in Figure 19. The combinational logic calculates if each bit should invert or not based on the conditions just described. The outputs of this block are registered, and they are updated in the falling edges of the *clk*. Therefore, once the counter changes its state there are 16 reference periods P_{ref} (or half clock period P_{clk}) until next state is registered to a[5:0]. In this time window the DCDL has to stabilize to the state, then the phase comparator has to generate the right *up* signal, and finally the next state logic of the counter has to calculate the next state. This is the most critical path of the system.

The registers bank is presented in Figure 20. The first bit always inverts its value, regardless of the value applied to **up**. The other bits invert or not depending on the results of the next state logic. This is realized with

Figure 19: Next state logic of the 7-bits counter.



Toggle flip-flops, which are implemented using a D flip-flop and a 2:1 multiplexer, as depicted in Figure 21. In order to asynchronously set $\overline{ctr}$ to 64, **preset** is connected to the reset of the first six flip-flops, and to the preset of the seventh flip-flop. Hence, when **preset** is high the word q[6:0] is set to 1 0 0 0 0 0 0.

Figure 20: Registers bank of the 7-bits counter.

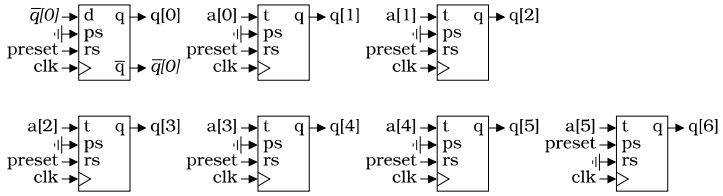
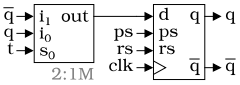
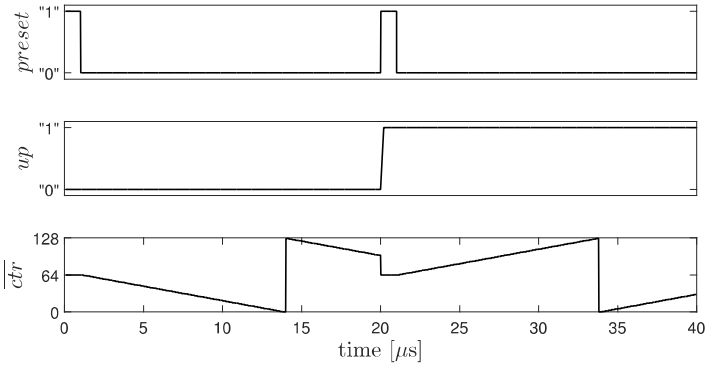


Figure 21: The implementation of the Toggle flip-flop used in the counter register bank.



The schematics of Figures 19 and 20 are a simplification of the circuits for visual purpose. The circuits that were implemented use standard CMOS logic gates (NOT, NOR, and NAND). The layout of the 7-bits accumulator is presented in Figure 63a, and its floorplan is depicted in Figure 63b in Appendix C.

Figure 22: Accumulator simulation result.



3.7.2 Simulation results

Figure 22 presents a typical operation of the counter. The input **oploop** is set to low, and therefore *ctr*[6:0] = *q*[6:0]. At the beginning of the operation *preset* is high, which forces $\overline{ctr}$ to 64. When *preset* turns to low, $\overline{ctr}$ start to decrease its value by 1 every clock period (P_{clk} = 200 ns). When $\overline{ctr}$ reaches 0, in the next rising edge of *clk* it turns to 127. When *preset* turns to high at 20 μs, $\overline{ctr}$ asynchronously change to 64. Then its value starts to increase by 1 once *preset* turns to low, because now *up* is high. When $\overline{ctr}$ reaches 127, in the next rising edge of *clk* it turns to 0.

3.8 DIGITAL CONTROLLED DELAY LINE

The DCDL is supplied with the core voltage V_{DDD} and has two inputs and one ouput at the same voltage rail. The inputs are:

- **in**: The signal applied to this pin is the digitized signal coming from the reference channel, i.e., *rch*.

- **c[6:0]**: The digital word applied to this bus controls the delay caused by the DCDL.

The output is:

- **out**: The signal flowing out of this pin is the delayed version of the signal applied to pin **in**. The amount of delay is controlled by the word applied to **c[6:0]**.

3.8.1 Topology

The DCDL is composed of seven delay blocks, and each delay block is composed of a number of cascaded delay elements (see Figure 8). The delay element is the building block of the DCDL, and the parameter that characterizes its variation in delay is δ. When the signal that controls the delay element changes from low to high, the delay of the signal passing through this element is incresed in δ seconds. The smaller the value of this parameter, the higher the resolution of the DLL.

The design criteria for the delay element were:

- To make δ as small as possible, in order to have the highest resolution;
- The delay element must use only standard logic gates and three state switches;
- The delay element must not invert the signal, only add δ seconds of delay;
- Its input impedance must be the same, regardless of the value of the control signal. This ensures that the time to charge or discharge the input node is always the same.

With these criteria in mind, we arrived at the topology presented in Figure 23 for the delay element. The circuit only uses inverters and three state switches. Both paths have an even number of cascaded inverters, which attends the criterion of not inverting the signal. The delay difference between one path and the other is the delay of two inverters, which is the minimum we can get without inverting the signal. And finally, the input impedance of the delay element is the input capacitance of two inverters, and does not change with the controlling signal.

The layout of one delay element is depicted in Figure 64a, and the floorplan is presented in Figure 64b. The layout of the whole DCDL is depicted in Figure 65a, and its floorplan is presented in Figure 65b. Figure 65c shows the power distribution network (thick solid line) and the signal flow (dashed line) in the DCDL.

Figure 23: Topology of one delay element.

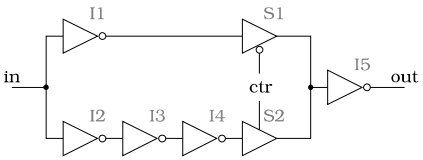


Table 2: Simulation results of one delay element.

	ctr = 0		ctr = 1		
corner	Δ_{t_r} [ps]	Δ_{t_f} [ps]	Δ_{t_r} [ps]	Δ_{t_f} [ps]	δ [ps]
tt	93.14	94.02	134.60	137.10	41.48
ff	66.61	67.56	96.58	98.75	29.97
ss	126.60	126.90	182.30	184.70	55.63
sf	98.46	94.17	140.90	138.00	42.43
fs	90.44	95.34	132.00	138.80	41.55
ssf	149.50	148.90	214.70	216.60	65.20
fff	59.60	60.37	86.52	88.39	26.92

3.8.2 Simulation Results

We start by simulating the delay element to obtain parameter δ. In order to simulate this circuit in the conditions it will operate in the DCDL, one delay element has to be connected before, and one after. Thus, the block we will measure the propagation delay is going to be loaded by the precedent delay element and then load the subsequent delay element (see Figure 8). Table 2 presents the simulation results of one delay element for each model corner of the used technology. The parameters in this table stand for:

- Δ_{t_r}: Time-delay between the rising edges of the input and output signals;
- Δ_{t_f}: Time-delay between the falling edges of the input and output signals;
- δ: Variation in the delay caused by the delay element when the control signal changes from low to high (i.e., $\delta = \Delta_{t_r}$[@ ctr = 1] - Δ_{t_r}[@ ctr = 0].)

Figure 24 presents the post-layout simulation results of the whole DCDL in the typical case (tt), and in the maximum and minimum delay sce-

Figure 24: Post-layout simulation result of the DCDL transfer function.

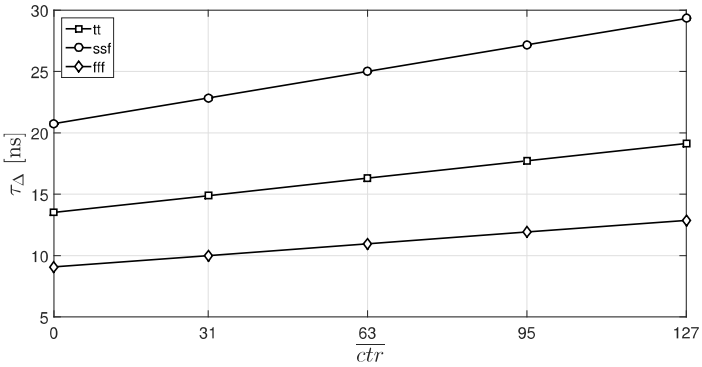


Table 3: Post-layout simulation results of the DCDL.

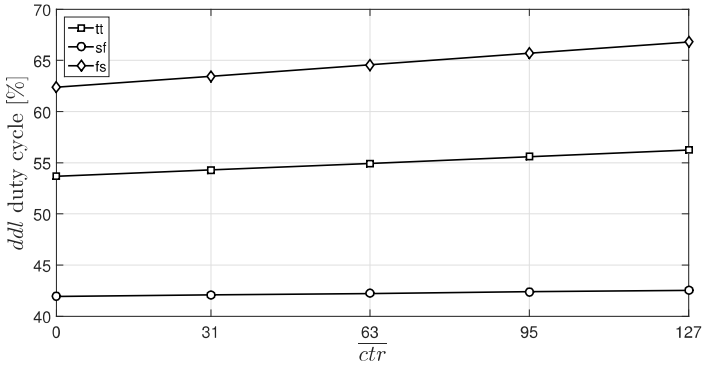
corner	δ ($\partial\tau_\Delta/\partial\overline{ctr}$) [ps/uc]	Range [ns]
tt	44.20	5.61
ssf	67.54	8.58
fff	29.80	3.78

narios (ssf and fff, respectively). Table 3 presents the slope of this curves, which is equivalent to the delay step δ[5]. This table also presents the range of delay covered by the DCDL, which equals δ times 127.

One major concern during the design of the DCDL was the output duty-cycle. Since the reference signal passes through hundreds of inverters, an imbalance in the threshold voltage of each inverter could reduce (or increase) the duty-cycle until the signal vanishes. For instance, if the inverter has a threshold above V_{DDD}/2 and a pulse is applied to it, the output pulse length is going to be slightly shorter than the input pulse length. If one connects enough inverters in series, eventually the pulse will disappear. To deal with this issue, we carefully designed the core inverter to have a threshold exactly at V_{DDD}/2 in the typical corner, and simulated the DCDL in the worse possible scenarios. Figure 25 depicts the duty-cycle of signal *ddl* when the DCDL input is 50 % duty-cycle. The worse corners in this case are sf and fs, which happen when one transistor is slow and the complementary is fast, and

[5]In the table "uc" stands for unit control, i.e., one unit of the digital word that controls the DCDL.

Figure 25: Post-layout simulation of the DCDL output duty-cycle for typical and worse scenarios.



vice-versa, because these are the corners that most affect the threshold. These simulation results show that the duty-cycle of the signal passing through the DCDL will vary with the model corners, but not enough for the signal to vanish.

The DCDL consumes a current of 1.26 mA from the V_{DDD} in the typical model corner. In corners ssf and fff, it consumes, respectively, 1.33 and 1.19 mA.

3.9 INPUT COMPARATORS

The input comparators are supplied with the IO voltage V_{DDA}, and have two analog inputs and one digital output. They are the only analog circuits in the system. The input (*inp* and *inn*) is an analog differential signal of 160 MHz, and the output is a digital single ended signal with the same frequency.

3.9.1 Topology

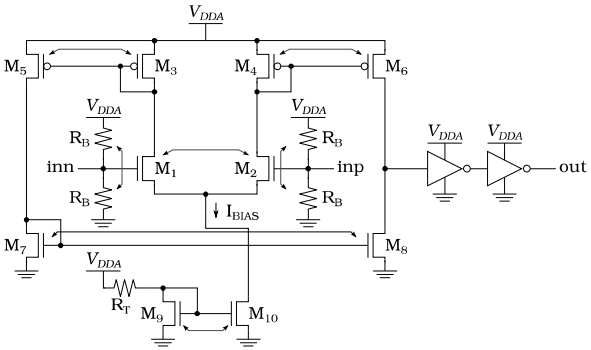
Figure 26 shows the circuit topology chosen for the input comparators. This topology is composed of a current-mirror operational amplifier (OpAmp) (JOHNS; MARTIN, 1997) and two inverters. This OpAmp has three interesting characteristics for our design: it is suitable for driving a ca-

pacitive load, the output node can swing rail-to-rail, and all internal nodes, except for the output, are low-impedance nodes. This last characteristic implies in negligible Miller effects, which makes this circuit a good choice for high frequency operation.

The design criteria for the input comparators were:

- For a sinusoidal differential input signal, the output must be a rail-to-rail square signal with 50 % duty-cycle in a typical scenario, and no more than $\pm 10\%$ variation in corner and Monte Carlo analysis;
- This sinusoidal signal can have an amplitude as low as 100 mV, and its frequency is 160 MHz;
- The simulation has to consider the ESD protections connected to the inputs of the comparators.

Figure 26: Input comparators topology.



The transistors aspect ratios and multiplicities are presented in Table 4. They were dimensioned through simulation, with the design criteria presented above as reference. The lengths of the differential pair transistors (M1 and M2) were set to minimum (0.4 μm) in order to reduce the input capacitance, and increase transconductance. The lengths of the other transistors were set to at least 1 μm in order to suppress channel modulation effects, therefore improving the current copy of the current-mirrors. The arrows show the devices that were interdigitezed in layout in order to reduce mismatch effects. All devices used in the input comparators are IO devices, since the supply rail is V_{DDA}.

The gates of the differential pair are internally biased with $V_{DDA}/2$, which is obtained with a resistive voltage divider. Each R_B is 6 serially con-

Table 4: Transistors dimensions of the input comparators.

Transistor	Multiplicity	W [μm]	L [μm]
M1, M2	12	6	0.4
M3, M4	5	6	1
M5, M6	4	6	1
M7, M8	5	1.25	1
M9	12	5	2.5
M10	24	5	2.5

Table 5: Output duty-cycle of the input comparator in corners.

	Corner				
Amplitude	**tt**	**sf**	**fs**	**ssf**	**fff**
50 mV	48.26 %	47.28 %	49.22 %	49.02 %	47.09 %
100 mV	50.24 %	49.63 %	50.85 %	50.82 %	49.51 %

nected 4 kΩ resistors (R_B = 24 kΩ). Therefore, each resistive voltage divider is composed of 12 resistors of 4 kΩ which are interdigitized in layout. The bias current I_{BIAS} was designed to 500 nA. The reference current is generated by resistor R_T whose value is 10.5 kΩ. The layout of one input comparator is presented in Figure 66, in Appendix C.

3.9.2 Simulation results

A differential signal v_{in} was applied to the inputs of the comparator (considering the ESD protections). This signal has a frequency of 160 MHz. Table 5 presents the corner results, and Table 6 the Monte Carlo results (process and mismatch, 100 runs) of the extracted view. The parameter measured in the simulations was the duty-cycle of the digital output signal for two amplitudes of the differential input signal: 100 mV, which was established in the design criteria, and 50 mV. In all scenarios the duty-cycle remained within the expected range.

Table 6: Output duty-cycle of the input comparator in Monte Carlo (100 runs, process and mismatch).

Amplitude	Mean	STDV
50 mV	48.39 %	2.44 %
100 mV	50.25 %	1.13 %

When driven with an input of 50 mV, each comparator consumes 1.43 mA in corner tt, 1.36 in ssf, and 1.19 in fff.

3.10 PARALLEL-TO-SERIAL CONVERTER

The parallel-to-serial converter is supplied with the core voltage V_{DDD} and has three inputs and one output. The inputs are:

- **pi[6:0]**: The 7-bits parallel word that is going to be serialized is applied to this input.
- **extclk**: The signal applied to this input determines the data rate of the output data stream.
- **reset**: When the signal applied to this input is high, the registers inside the P2S block are reseted and the output stays in low level.

The output is:

- **so**: A serial data stream. Each 8 bits form one word, where the 7 first bits are *ctr*[6:0] (from MSB to LSB) and the last is always 0.

3.10.1 Topology

The topology adopted for the parallel-to-serial converter is depicted in Figure 27. It is composed of a register bank (RB), a frequency divider (FDIV), and an 8:1 multiplexer. The frequency divider divides *clk* by 2, 4, and 8. Its topology is equal to that of the frequency divider presented in Figure 17, but with only three stages, and one output per stage. It also has an additional input signal *reset* which asynchronously resets the frequency divider.

The frequency divider acts as a down-counter, where the outputs *div8*, *div4*, and *div2* form a digital word that starts in 1 1 1 and decreases by 1 at each rising edge of *extclk*, see Figure 28. When the word reaches 0 0 0, it returns to 1 1 1. This word determines which input of the 8:1 MUX will be transmitted to the output *so*. The input word *pi*[6:0] is loaded in the register bank at each 8 pulses of *extclk*, i.e., at every rising edge of the signal *div8*. Figure 28 illustrates the operation of the P2S block.

The *reset* signal serves to synchronize the output data stream with the *extclk* pulses. After a reset, the first *extclk* rising edge is going to send the

signal *pi[6]* to the output, and then *pi[5]*, *pi[4]*, *pi[3]*, *pi[1]*, *pi[0]*, and '0'. Then the process starts again with a new input word loaded to the register bank.

The layout of the P2S block and its floorplan are depicted in Figures 67a and 67b, in Appendix C.

Figure 27: Topology of the parallel-to-serial converter.

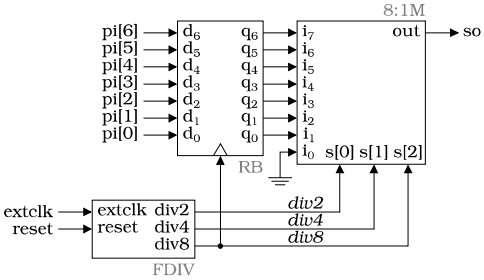
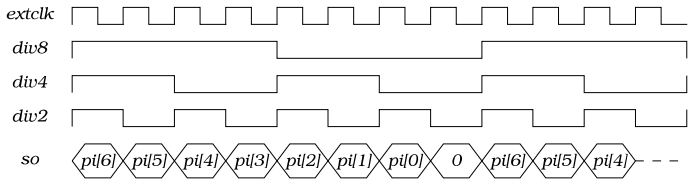


Figure 28: P2S typical operation.



3.11 TEST MULTIPLEXER

The test multiplexer is supplied with the core voltage V_{DDD} and has one digital input word of three bits **s[2:0]**, other eight digital inputs **i_0** to **i_7**, and one digital output **out**. The input word controls which one of the eight inputs is transmitted to the output. This block is simply a multiplexer 8:1, and its inputs are internal signals we wish to measure for testing and debugging purposes. Table 7 presents the test multiplexer truth table. The layout of the test multiplexer is presented in Figure 58 of Appendix C.

Table 7: Test multiplexer truth table.

s[2:0]	Position	Output signal
0 0 0	0	*ddl*
0 0 1	1	*rch*
0 1 0	2	*sch*
0 1 1	3	*up*
1 0 0	4	*clk*
1 0 1	5	*div8*
1 1 0	6	*div4*
1 1 1	7	*div2*

3.12 SYSTEM INTEGRATION

All the connections between the individual blocks were carefully planned and designed to avoid fan-out issues. Big capacitors (C_{si} = 84 pF) were added between each supply rail and ground in order to filter supply noise. The final design contains 25 pads, 23 of them are depicted in Figure 10, plus two additional pads for **GND** and **VDDA**. The integrated circuits is packed in an OCP_SOIC_300_28A (Open Cavity Plastic, Small Outline Integrated Circuit, 28 pins). The additional 3 pads were used in another project.

3.12.1 Layout

The layout of the whole system is presented in Figure 30a, and its floorplan is presented in Figure 30b. Figure 31 shows a photography of the packaged IC. The layouts of the individual blocks are presented in Appendix C. The total design area is 570 μm by 760 μm, or 0.433 mm^2. The area disregarding the ESD protections and the supply capacitors is 370 μm by 200 μm, or 0.074 mm^2.

The routing of internal signals was realized with the 3 bottom-most levels of metal. Each level has paths orthogonal to the paths of the predecessor level, which facilitates routing, specially in the digital blocks. The 4 top-most levels of metal were used for power distribution, because they are less resistive (more thick) than the bottom ones, and they can support a higher current density. These metals are also used to connect IO devices to pads.

Guard rings with contacts to substrate were used in order to better isolate the main blocks. These guard rings reduce the substrate resistance and

also provide a path to ground to the substrate currents, considerably reducing the noise between the blocks. The DCDL, for instance, is suspected to be a very noisy block, because hundreds of inverters will be switching within only one reference period, and not at the same time. Therefore, a thick guard ring surrounds this block (see Figures 65a and 65b). Besides that, each delay element has a lot of contacts to substrate (see Figure 64).

3.12.2 Simulation Results

The individual blocks were simulated stand-alone in post-layout and model corners (when judged necessary). We focused on obtaining the desired behavior for each individual block, and also on guaranteeing the right connectivity between them. The simulation of a whole DLL is very time consuming, because there are two very separated time constants, the reference period, which is 6.25 ns, and the update (clock) period, which is 200 ns. This is similar to the simulation of PLL (Phase-locked loops). Since we did not have closed specifications to fulfill, the whole system was simulated only to verify connectivity and possible layout issues.

Figure 29: Post-layout simulation of the whole DLL.

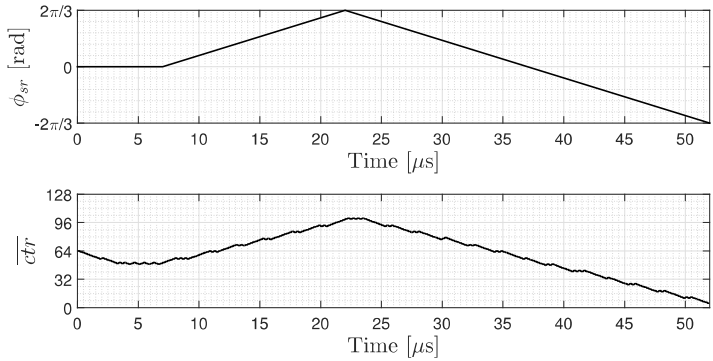


Figure 29 presents the post-layout simulation results of the whole DLL in the typical model corner. In this simulation, the phase ϕ_{sr} between signals *sch* and *rch*[6] starts in 0, then linearly increases to $2\pi/3$, and then linearly

[6] A positive phase means signal *sch* is delayed in relation to *rch*

Table 8: Estimated power consumption.

	tt	**ssf**	**fff**
I_{DDA} [mA]	2.93	2.79	3.09
I_{DDD} [mA]	1.30	1.37	1.23
P_{DC} [mW]	11.23	10.85	11.67

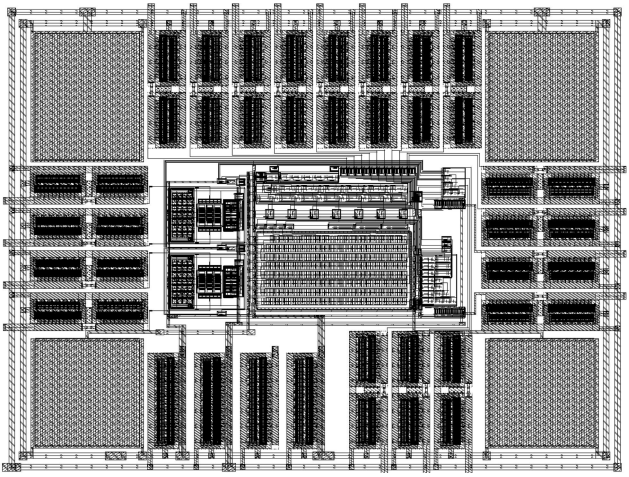
decreases to -2π/3. Variations in this phase caused by the SAW-DL interacting with the measurand will be much slower than the values used here. We use this fast transitions to save simulation time. As we can see, the value of the control word follows the phase difference, which is equivalent to delay difference, as expected.

Table 8 presents the estimated current and power consumptions for models corners tt, ssf, and fff. The average currents drawn from the IO and core voltage rails are, respectively, I_{DDA} and I_{DDD}, and P_{DC}[7] is the total DC power. This estimation considers that the input comparators are driven with a signal of 50 mV of amplitude, the output buffers are driving a signal of 5 MHz in a 1 pF capacitor. The two most power hungry blocks are the ICMP and the DCDL.

[7] $P_{DC} = I_{DDA}V_{DDA} + I_{DDD}V_{DDD}$

Figure 30: Layout of the whole system.

(a) Layout



(b) Floorplan

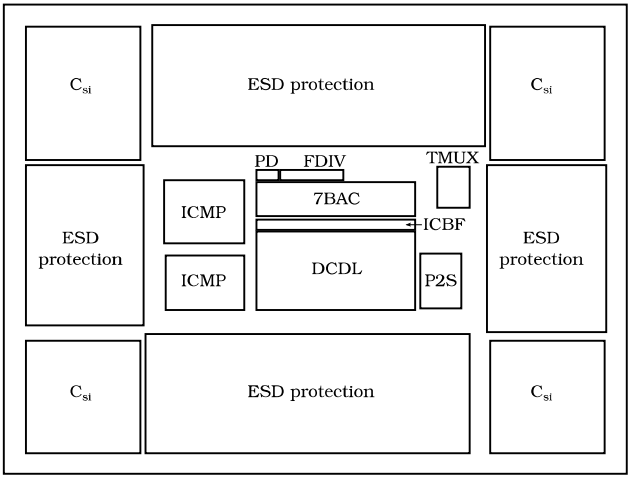
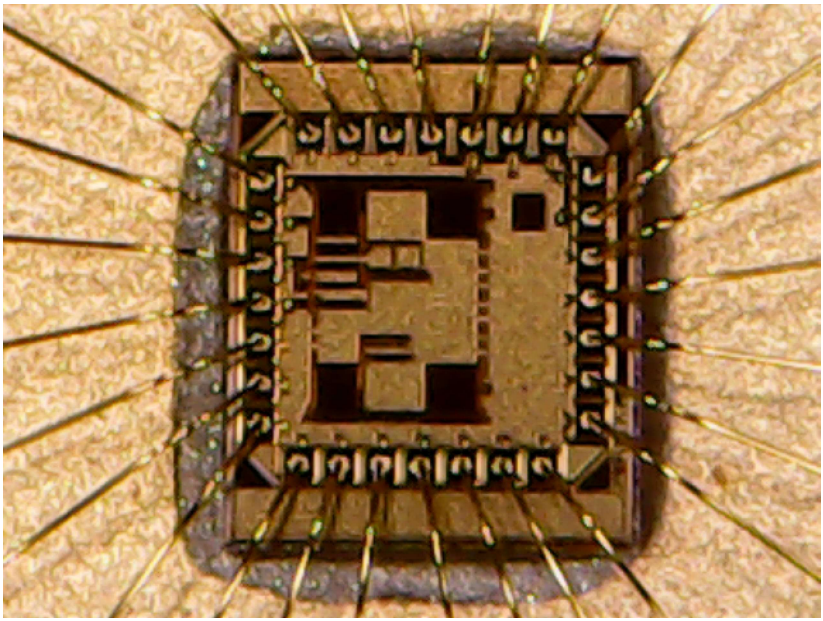


Figure 31: Photography of the packaged IC.



4 MEASUREMENTS OF THE DESIGNED CONDITIONER

This chapter is dedicated to the measurement of the designed prototype. The tests are divided into two sections, the functional tests, which comprise the measurement of the conditioner stand-alone, and the humidity tests, which comprise the measurement of the proposed setup to measure RH.

4.1 TEST BOARDS AND EQUIPMENTS

This section presents the test boards and equipments used in the following measurement setups.

4.1.1 Test Boards

Two test boards were used in the measurement of our system. Test Board 1 (TB1) is used in the functional tests and in the humidity tests, and it is presented in Figure 32. With this board we can externally control the state of the accumulator through switches DIP1. We can also configure the output of the test multiplexer through switches DIP2. Resistors R_P of 100 kΩ serve to pull-down the node when the corresponding switch is open. Resistor R_C of 5.1 kΩ serves to smooth the transition edges of the square signal applied as external clock. Capacitors C_B of 1 nF are bypass capacitors to isolate the DC component and let the 160 MHz signal pass. The high frequency signals are coupled to the board through SMA connectors (**SMA1** comes from the sensing channel, and **SMA2** from the reference). The power supplies are coupled to the board through the bourne **B1**. Capacitors C_S of 100 nF (ceramic) in parallel with 33 μF (electrolytic) are used to filter the supply noise. The button S_1 is used to generate the reset signal.

Test Board 2 (TB2) is presented in Figure 33. This board is used only in the humidity tests, in order to test a second sample of the integrated circuit. Therefore, there is no need to configure the test multiplexer, or to apply an external control word. Hence, the test multiplexer input **TMUX[2:0]** is hardwired to position 4, and pins **OPLOOP** and **EXTCTR[6:0]** are grounded. TB2 is a simplified version of TB1. We chose to simplify it in order to reduce the board size, and also because the reconfigurability of TB1 was not required after the system was operating correctly.

Figures 34 and 35 present photographies of TB1 and TB2, respecti-

vely.

Figure 32: Test Board 1.

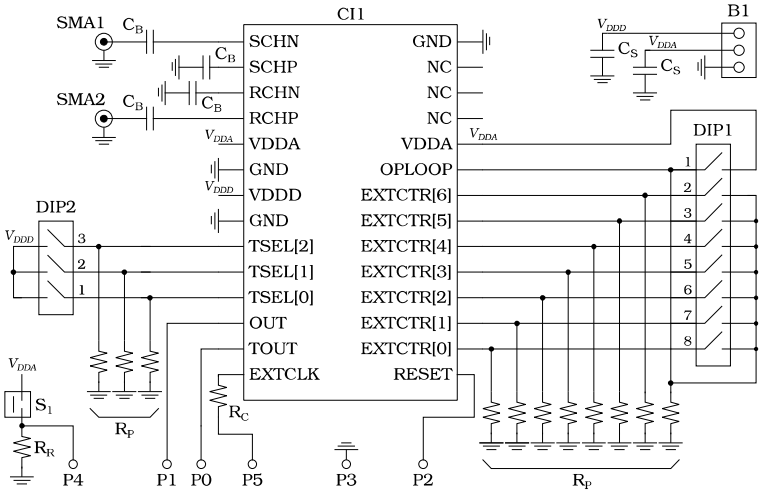


Figure 33: Test Board 2.

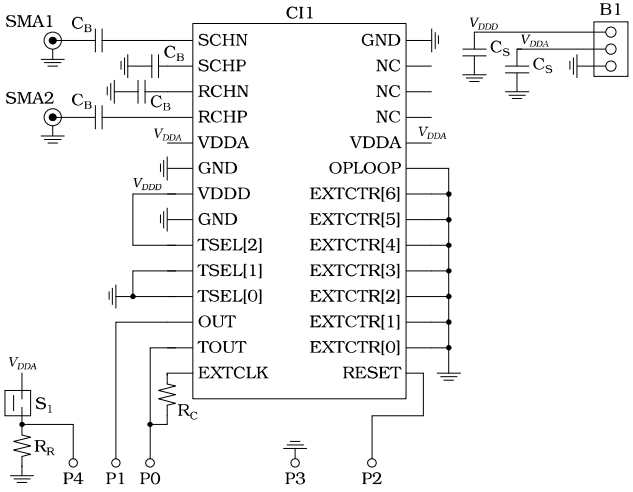


Figure 34: TB1 photography.

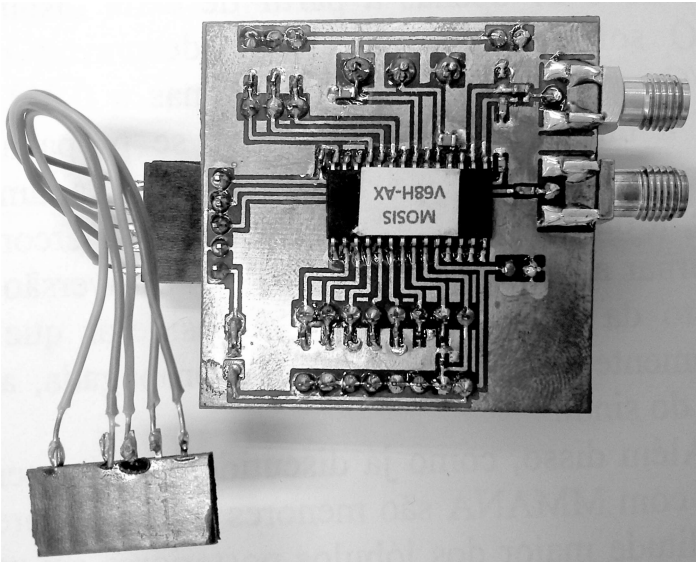
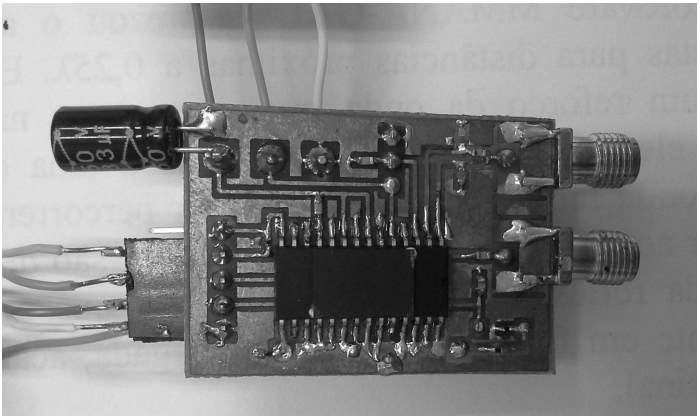


Figure 35: TB2 photography.



4.1.2 Equipaments

Oscilloscope: DSO-X 2014A of Agilent Technologies. All voltage probes are N2862B 10:1 passive probes with a parallel capacitance of 15 pF and series resistance of 10 MΩ. It is possible to save csv files with a resolution of 50 thousand points in a window of 200 μs. The bandwidth limitation (20 MHz) was enabled in all channels and during all experiments, in order to suppress high-frequency noise. This oscilloscope has the function "Single", which takes one shot in the event of a trigger.

DC source: PS-7000 of Icel. This DC source supplies 5 V to the regulators that generate V_{DDD} and V_{DDA}.

Signal source 1: 33220A of Agilent Technologies. This signal source is used to generate reference signals of 1 and 5 MHz for functional test purposes. The main output has a 50 Ω output impedance. The sync output generates a square signal from 0 to 3.3 V synchronized in phase to the main output signal. This information is important for the DCDL functional test.

Signal source 2: USRP B210 of Ettus Research. This SDR board is configured to generate two sinusoidal signals of 160 MHz whose phase-difference can be set via computer interface. The amplitude of both signals is also set via computer interface by variable "gain". These two signals are applied directly to the test boards (**SMA1** and **SMA2**) in order to perform the functional tests, or to the sense and reference SAW devices in order to perform the humidity tests. The relation between variable "gain" and the power delivered to a 50-Ω load in the frequency of interest is presented in Appendix B.1.

FPGA development board: DE0-Nano of Terasic. This board is used to generate a reset signal synchronized to the falling edge of the clock. The signal in **P4** is registered in the falling edges of the signal in **P0** (test multiplexer configured to position 4). The output of the register is then applied to **P2**. This is necessary for a synchronization of the data. The code installed in the DE0-Nano board is presented in Appendix A.1.

4.2 FUNCTIONAL TESTS

This section is dedicated to the conditioner stand-alone functional verifications.

4.2.1 Internal clock

Purpose: To measure the internal clock signal (*clk*), which determines the DLL update rate. This signal is generated by frequency-dividing *sch* by 32, which shall result in a signal of 5 MHz.

Test Bench: This measurement is performed with Test Board 1. A signal of 160 MHz and amplitude determined by variable "gain" is generated by the USRP board and applied to the input **SMA1** through a coaxial cable. The test multiplexer is configured to position 4, which outputs the internal signal *clk*. Channel 1 of the oscilloscope is connected to pin **P0**.

Results: Figures 36a and 36b present the oscilloscope frames for two values of "gain", 33 and 40, respectively. For the first value, and values below, the internal clock is not generated correctly. For a "gain" of 35 and above the signal is a periodic square wave[1] of 5 MHz, as expected. Throughout the rest of the functional measurements "gain" is set to 40.

4.2.2 External clock division

Purpose: To verify if the signal applied to pin **EXTCLK** is being correctly divide by 2, 4, and 8 in the parallel-to-serial converter.

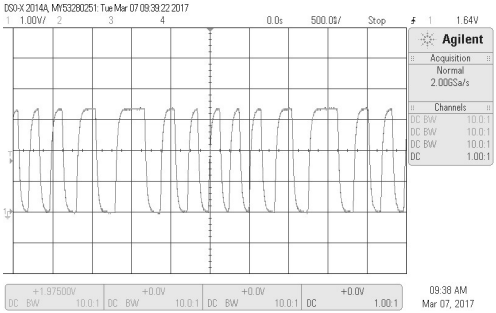
Test Bench: This measurement is performed with Test Board 1. A square signal from 0 V to 3.3 V, frequency of 5 MHz and 50 % duty cycle is applied to **P5**. Resistor R_C has the function of smoothing the transitions of the signal that arrives in **EXTCLK**. This is necessary because steep transitions generate a lot of noise, which impacts in the DLL performance. In order to measure *div2*, *div4*, and *div8*, the test multiplexer must be configured to positions 7, 6, and 5, respectively (see Table 7). In this measurement it is fundamental that pin **P2** (**RESET**) is grounded, otherwise the divisions will not be performed correctly. Channel 1 of the oscilloscope is connected to **P5**, and channel 2 to **P0**.

Results: Figures 37a, 37b, and 37c present the measurements of signals *div2*, *div4*, and *div8*, through the test multiplexer. All the frequency divisions were performed correctly.

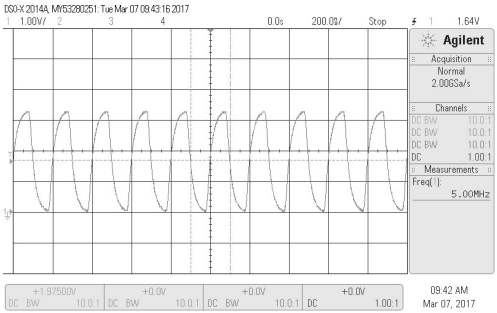
[1] The slow transitions in this signals are caused by the low-pass filter formed by the ESD protection circuit and the voltage probe capacitance.

Figure 36: Internal clock signal.

(a) "gain" = 33.



(b) "gain" = 40.



4.2.3 Output data stream

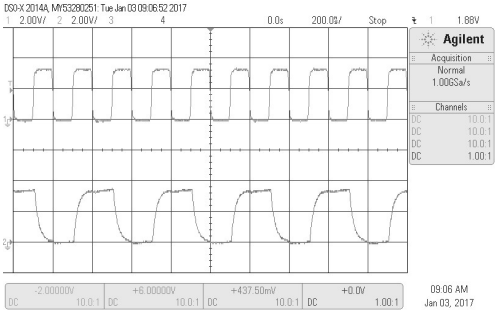
Purpose: To verify if the P2S block is correctly converting the internal word *ctr*[6:0] to a data stream.

Test Bench: This measurement is performed with Test Board 1. From now on, the internal clock (*clk*) of 5 MHz is going to be applied to **EXTCLK** in order to pace the P2S block[2]. In order to do that, pins **P0** and **P5** are shorted, and the test multiplexer is configured to position 4. A signal of 160 MHz and "gain" = 40 is generated by the USRP board and applied to the input

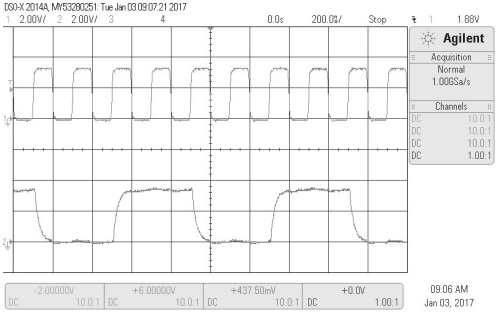
[2]If the clock applied to **EXTCLK** is not synchronized to *clk*, the registers of the P2S block can sample the word *ctr*[6:0] in a moment it is transitioning, therefore generating a wrong result. By using *clk* to pace the P2S block, we avoid this wrong behavior

Figure 37: External clock division.

(a) Division by 2.



(b) Division by 4.



(c) Division by 8.

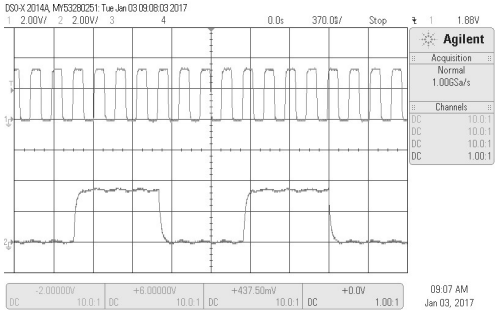
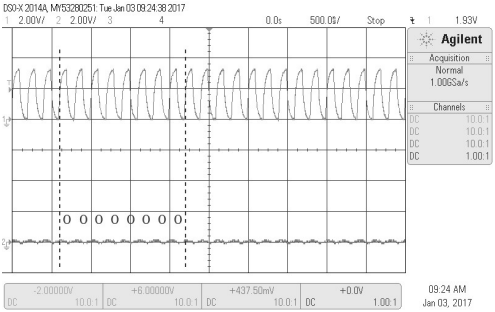
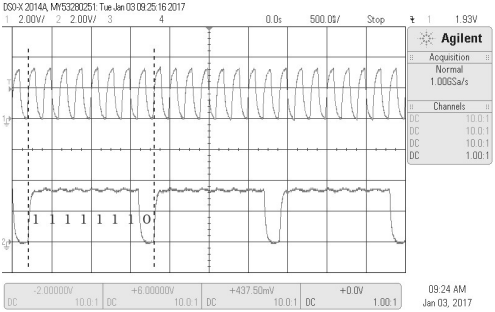


Figure 38: Output data stream.

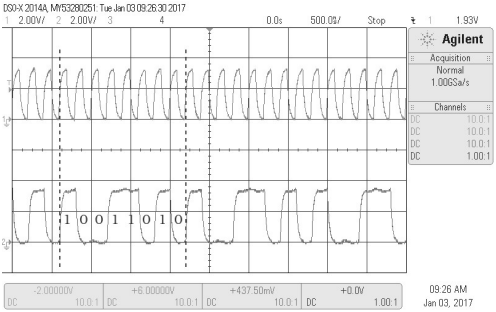
(a) EXTCTR[6:0] = 0 0 0 0 0 0 0.



(b) EXTCTR[6:0] = 1 1 1 1 1 1 1.



(c) EXTCTR[6:0] = 1 0 0 1 1 0 1.



SMA1. The DLL loop is opened by closing switch 1 of DIP1, and external words are forced by configuring switches 2 to 8 of DIP1. Three external words were used: 0 0 0 0 0 0 0, 1 1 1 1 1 1 1, and 1 0 0 1 1 0 1. Channel 1 of the oscilloscope is connected to **P0**, and channel 2 to **P1**.

Results: Figures 38a, 38b, and 38c present the oscilloscope windows for the three words applied to **EXTCTR[6:0]**: 0 0 0 0 0 0 0, 1 1 1 1 1 1 1, and 1 0 0 1 1 0 1. The parallel-to-serial conversion is being correctly performed. Notice that the last bit is always 0, because of the architecture of the P2S block (see Figure 27).

4.2.4 DCDL

Purpose: To verify the correct operation of the Digital-Controlled Delay Line (DCDL), and to estimate the transfer function of this block.

Test Bench: This measurement is performed with Test Board 1. A sinusoidal signal of 1 MHz and amplitude of 100 mV (peak-to-peak) is applied to **SMA2**. The test multiplexer is configured to position 0, which outputs the signal *ddl*, the output of the DCDL. The DLL loop is opened by closing switch 1 of DIP1, and external words are forced by configuring switches 2 to 8 of DIP1. Channel 1 of the oscilloscope is connected to **P0**, and channel 2 to the sync output of the signal source. The oscilloscope window is configured to display the rising edges of the signals, in order to measure the time-delay between them. An average operation of 4096 points is applied to both channels in order to suppress noise in the transitions.

Results: Figures 39a, 39b, and 39c depict the oscilloscope windows for three values of the external word 0, 64, and 127, respectively. Notice the parameter ΔX that represents the time-delay between the rising edges. Figure 40 presents a graphic of this delay versus the applied word for three measurements. By taking the average of the three measurements for each word value and then making a linear regression[3] we obtain the dashed curve. The slope of this curve is 58.7 ps/uc. By comparing this result with the simulation of the DCDL presented in Tables 2 and 3 we can infer that either the integrated circuit being measured is in between corners ss and ssf, i.e., both transistors are slower than the typical devices, or the parasitic capacitances were underestimated by the parasitic extraction tool.

Since the gain of the DLL is inversely related to the gain of the DCDL

[3] With function polyfit in Octave.

(see Equation 19), a higher value of δ[4] implies in a smaller variation in the value of the output word for the same amount of delay. In order to measure the response of our conditioner with a higher DLL gain, we decided to boost the DCDL by increasing the value of V_{DDD} to 1.8 V in some measurements. Figure 41 presents a graphic of this delay versus the applied word for the boosted DCDL. The slope of the linear regression curve in this case is 32.9 ps/uc.

4.2.5 DLL

Purpose: To measure the response of the DLL to external perturbations. The result of this test is a curve of the output word value versus the phase difference between the reference and the sensing channels. From this curve one can extract parameter δ, the delay step of the DCDL.

Test Bench: This measurement is performed with both test boards. For TB1, the test multiplexer must be configured to position 4 through switches DIP2, and pins **P0** and **P5** must be shorted. The test bench is presented in Figure 42. A PC is used to program the USRP and the DE0-Nano boards. The output channels of the USRP board are connected to **SMA1** and **SMA2** of the test board through coaxial cables of the same length (approximately 20 cm). Parameter "gain" is set to 40. The DE0-Nano board is programmed with the code presented in Appendix A.1. Channel 1 of the oscilloscope measures the clock signal, channel 2 the output data stream, and channel 3 the reset signal.

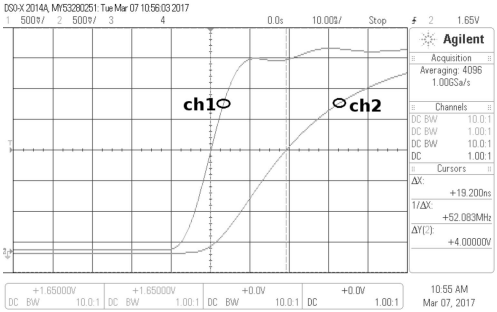
Data Acquisition and Analysis: In order to decode the output data stream, we need to acquire and process three signals: the data, the clock, and the reset (used to synchronize). Figure 43 presents an example of the acquisition of these signals in the oscilloscope. The trigger was set to the falling edges of channel 3, which measures the reset signal, crossing 1.65 V (V_{DDA}/2). Then, we used the oscilloscope function "Single" and press the reset button S_1. After stop pressing the button, the oscilloscope acquires one frame and freezes it. In order to get the frame presented in Figure 43, the window size was configured to 500 μs, and the trigger offset to 240 μs. Each frame contains around 306 words[5]. The data of each frame is saved as a csv file with a resolution of 10000 points.

[4] Compared to the typical case.

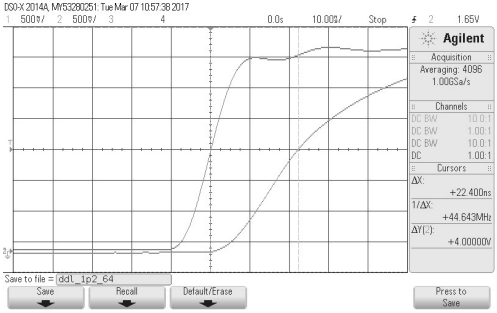
[5] Each word has a length of 8 clock periods of 200 ns. The frame, disregarding the period in which reset is high, has a length of 490 μs.

Figure 39: Measurement of the delay caused by the DCDL.

(a) External word set to 0.



(b) External word set to 64.



(c) External word set to 127.

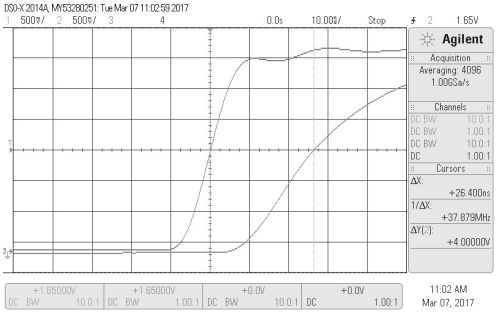


Figure 40: Measurement of the DCDL transfer function for V_{DDD} = 1.2 V.

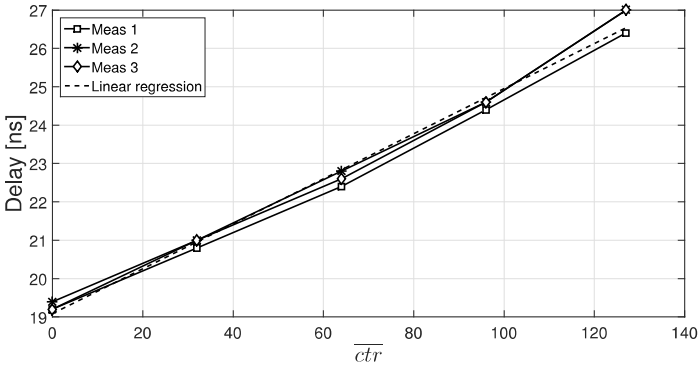
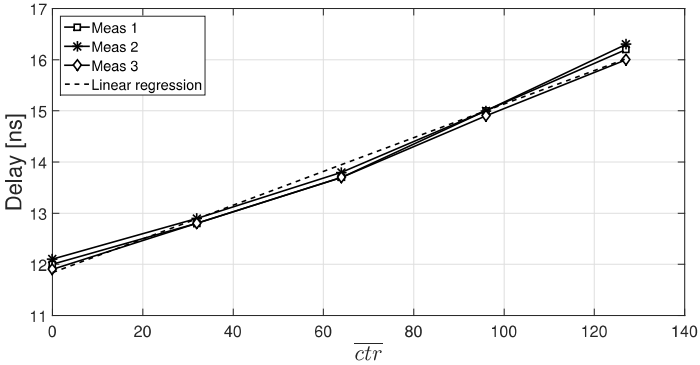
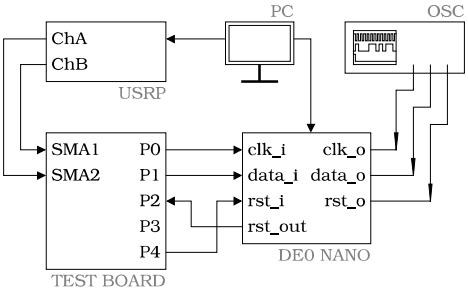


Figure 41: Measurement of the DCDL transfer function for V_{DDD} = 1.8 V.



The csv file is analyzed with the Octave function presented in Appendix A.2. This function receives the data of one frame, and returns an array with the decimal values of the serial words in this frame. Since the reset button is pressed every time we want to get a new frame, it takes a few words for the DLL to stabilize. We can disregard these transient words by setting the initial point in the array returned by the function. For the present test, the first 20 words were disregarded. Then, we take the average of the values in the array. Therefore, one frame results in a number, which is the average value of

Figure 42: Test bench schematic for measuring the DLL response.



the output words disregarding the transient. For a further explanation of the function, please read Appendix A.2.

Results: Figures 44a and 44b present the test results for TB1, with V_{DDD} of 1.2 and 1.8 V, respectively. The equivalent results for TB2 are presented in Figures 45a and 45b. The x axis represents the phase between the signals generated by the USRP board and applied to **SMA1** and **SMA2**. The y axis represents an estimation of the word value, denoted by $\widehat{ctr}$. Each square marker in the graphics represents the average of 10 data frames. In other words, for each value of phase we took 10 frames, which resulted in 10 numbers, and then we took the average of these numbers[6]. The averages as well as the normal standard deviations for each point in the four graphics are presented in the additional test results section, Appendix B.2.

Let us put aside, for a moment, the points that are out of the ramp

[6]It is worth notice that even though the digital words in the output of our system can only assume integer values, the results here can be fractional, because we are taking two averages. The first is in the processing of one frame, and the second in 10 processed frames.

Figure 43: Example of one data frame acquired in the oscilloscope.

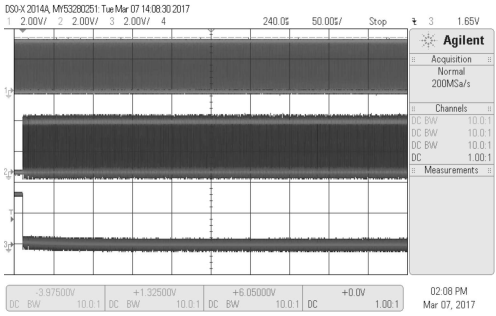
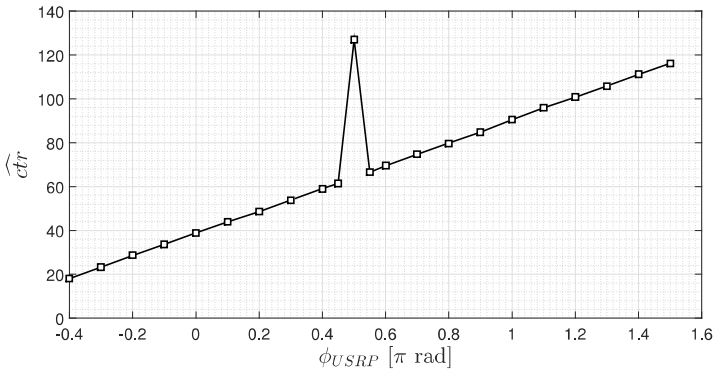
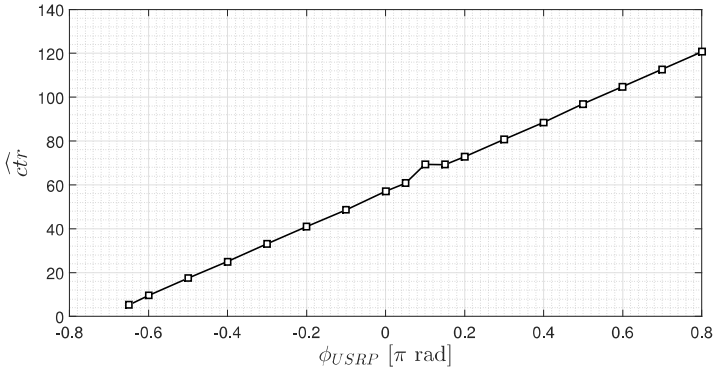


Figure 44: TB1 DLL response.

(a) V_{DDD} **= 1.2 V.**



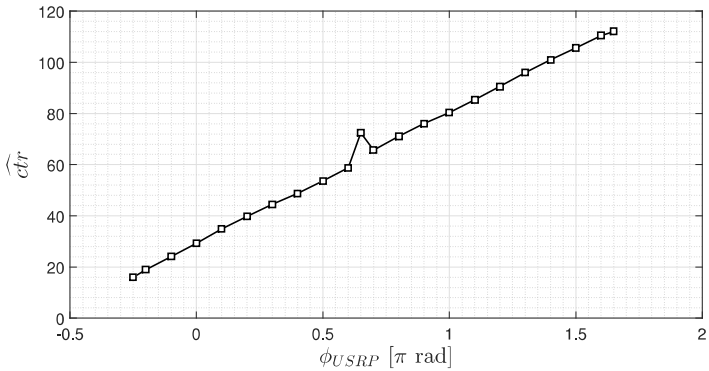
(b) V_{DDD} **= 1.8 V.**



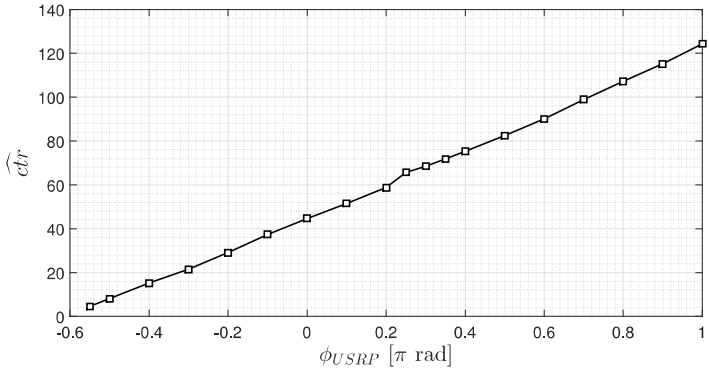
in the graphics (in all cases when $\widehat{ctr}$ is close to 64). The system responds nearly linear to phase variations between the signals applied to the reference and sensing channels, as we expected. For a V_{DDD} of 1.2 V, the DCDL covers more then one reference period (P_{ref} = 6.25 ns, see Figure 40). Therefore, since we restart the system each time a new frame is captured, it is not possible to reach values close to 0 and 127. For instance, if we set the phase to -0.5 π rad in Figure 44a, the result will be the same as if the phase was 1.5 π

Figure 45: TB2 DLL response.

(a) V_{DDD} **= 1.2 V.**



(b) V_{DDD} **= 1.8 V.**



rad. For a V_{DDD} of 1.8 V, the DCDL does not cover an entire reference period (see Figure 41). This allows a full measurement of the DLL response.

The slopes of the curves, which represent the estimated DLL gain, as well as the corresponding δ values, are presented in Table 9. In order to calculate the slope of a curve, the point that is out of the ramp was not considered. The calculation is realized by the Octave function *polyfit*, which returns the coefficients of a polynomial (of the first order, in this case) that minimizes

Table 9: Estimated DLL gain and δ.

	V_{DDD}	**Inclination [/ π rad]**	**δ [ps/uc]**
TB1	1.2 V	51.68	60.46
	1.8 V	79.53	39.29
TB2	1.2 V	50.99	61.29
	1.8 V	76.84	40.67

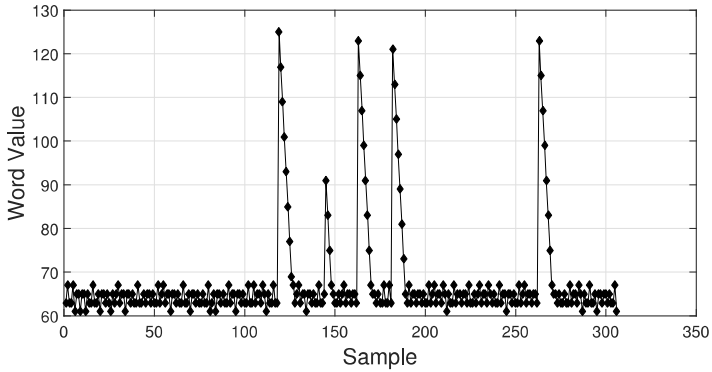
the least-square error between the data and the polynomial. By comparing Tables 9 and 2, we can conclude that both tested chips are close to the ssf model corner, i.e., both transistors are very slow. This is the worse corner for our system, because it makes δ too big, which decreases the responsivity. By increasing the core voltage V_{DDD} to 1.8 V, the value of δ gets closer to the tt model corner.

Notice that the values of δ obtained in this test for TB1 are slightly different than the ones obtained in Section 4.2.4. We believe this difference is due to the fact that in the test of Section 4.2.4 the oscilloscope bars used to measure the delay in the rising edge were set manually. Therefore, the values of δ presented in Table 9 are more reliable than the ones presented in the last section.

Now let us take a look to the response when it crosses 64. Figure 46 presents one of the ten frames (before the first average) used to calculate 0.1 π rad in Figure 44b. The system stabilizes around 64, but from time to time it jumps to a higher value and then returns to 64. This happens because the *up* signal changes during a falling edge of the *clk* (see Section 3.7 for a visual representation of the accumulator). For instance, if the value of the word *ctr*[6:0] is 0 1 1 1 1 1 1 (63), and *up* is high the next value of the word must be 1 0 0 0 0 0 0 (64). However, if *up* transitions close to a falling edge of *clk* in such a way that there is not enough time for the next state logic to stabilize (see Figure 19), the accumulator state might change to 1 1 1 1 1 1 1 (127).

It was not expected that *up* would transition once the system had stabilized in a new state. This is because the phase-noise of the reference signal was not considered in our simulations. In future designs we recommend that signal *up* is registered in a flip-flop before the falling edge of *clk*, in order to prevent a wrong calculation of the next state. Fortunately, this issue did not prevent the humidity measurements in the next section.

Figure 46: One frame used to calculate 0.1 π rad in Figure 44b.



4.2.6 Current consumption

Purpose: To determine the current consumption of the system during a typical operation.

Test Bench: This test is performed with both test boards. For TB1, the test multiplexer must be configured to position 4 through switches DIP2, and pins **P0** and **P5** must be shorted. The test bench is the same as in the previous measurement, except for the oscilloscope which does not need to be connected. An ammeter measures the currents entering bourne B_1 in the test boards. Parameter "gain" of the USRP is set to 40.

Results: Tables 10 and 11 summarize the current consumption of the two test boards, and for the two values of V_{DDD}. If we compare Tables 10 and 8 we notice an increase in the measured currents in relation to what was expected in simulation. Further simulations were realized, however we did not find the source of this difference.

Table 10: Current consumption for V_{DDD} = 1.2 V.

	I_{DDD} (mA)	I_{DDA} (mA)
TB1	1.70	3.30
TB2	1.70	3.33

Table 11: Current consumption for V_{DDD} = 1.8 V.

	I_{DDD} **(mA)**	I_{DDA} **(mA)**
TB1	2.55	3.32
TB2	2.54	3.32

4.3 HUMIDITY TESTS

This section presents the measurement results of the proposed setup to measure RH, composed of the conditioner and the SAW devices.

4.3.1 Humidity control

Saturated saline solutions (SSS) are widely used to control the RH of small environments in laboratory experiments, containers that store and transport special materials, and also to calibrate humidity sensors (GREENSPAN, 1977). In our experiment, we made use of four SSSs: Magnesium Chloride ($MgCl_2$), Magnesium Nitrate ($Mg(NO_3)_2$), Sodium Chloride (NaCl), and Barium Chloride ($BaCl_2$). At 25 °C and normal atmospheric pressure, these solutions bring the RH of the environment in which they are contained to, respectively: 32.8 %, 52.9 %, 75.3 %, and 90.0 %. The solutions were prepared using distilled water and the salts in their pure form. If the solutions are correctly prepared, they bring the RH to the specified values with very small error, and that is why they are used as standard for calibrating humidity sensors.

A kitchen container of 1400 mL was used to create a sealed environment. The SAW devices (reference and sensing channels) were fixed on the walls of the container using hot glue, taking care as to not leave any passage of air. Previous to this modification, we added water inside the container, closed it with its lid, and turned it upside down to check if there were any leakage. None was found. We concluded that the container had a fairly good humidity isolation. The solutions were placed inside the container, one at a time, in order to control the RH to the desired value.

4.3.2 Temperature Control

We do not know exactly what is the influence of the temperature in our system. We believe that the reference channel can compensate for temperature variations when both devices are fabricated over the same substrate. However, here we have two separate devices, soldered in different PCBs, and with a distance between them. Moreover, our circuitry was not designed to be temperature compensated. Therefore, it is out of the scope of this work to determine the influence of temperature in the performance of our system.

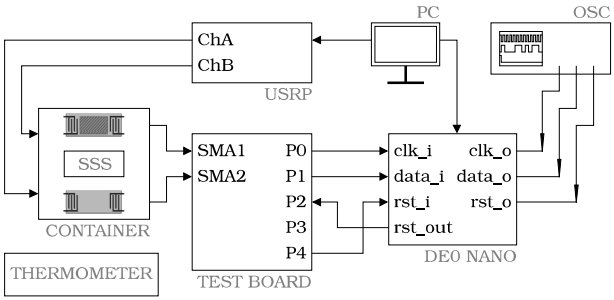
When the laboratory air-conditioner was set to a fixed temperature value, we noticed a high fluctuation in temperature (>3 °C) throughout one day. In order to reduce this fluctuation, the control was realized manually, by turning up or down the air-conditioner, and by maintaining the room always closed. The temperature was measured with a thermometer (J.Prolab 1566-1) positioned outside the container.

4.3.3 Test Bench

The test bench used for the humidity tests is presented in Figure 47. The USRP channels are connected to the SAW devices through coaxial cables of the same length (60 cm). The other port of each SAW device is connected to the test board also through coaxial cables of the same length (60 cm). The remaining connections are equal to the ones in the test bench used in Section 4.2.4 for extracting the DLL response curve. The phase between the USRP channels was set to 0 radians throughout the whole experiment. The parameter "gain" of the USRP was increased to 60, to account for the SAW devices attenuation. The data acquisition and analysis is also the same as in Section 4.2.4, except that now the oscilloscope is configured with a window length of 2000 μs, and a trigger offset of 990 μs. Therefore, now each frame has 1243 words.

When we started the humidity tests, we connected the USRP, container, and test board with flexible coaxial cables. This resulted in large variations in the mean value of frames taken consecutively in the same humidity conditions. Since we are measuring delays in the order of tens of picoseconds (δ is around 40 to 60 ps), any small movements in the cables could

Figure 47: Test bench used to measure RH.

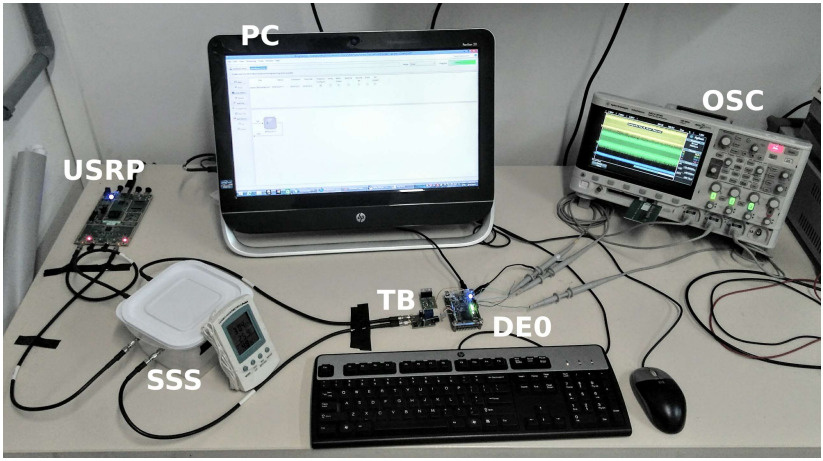


considerably change the delay of one or both of the signal paths. In order to circumvent this problem, we first tried to fix the cables in the table with tapes. By doing so, consecutive frames presented a much shorter variation in their mean value. However, when we tried to replicate the same results (same RH condition) with an interval of a day, or even hours, we noticed considerable variations in the mean value of the frames. The final solution was to replace the flexible cables by rigid ones, which could roughly maintain their position throughout the whole test, and avoid hitting or moving or shaking the test bench. Ideally, the signal generator, the SAW devices, and the conditioner should be mounted on the same PCB, to avoid the use of cables.

The same problem happened with the container. At first we let it unfixed on the table. Every time the solution had to be changed, in order to stabilize the RH to another level, the container was shaken and slightly moved. Therefore, it had to be fixed on the table with double-sided tape. We also avoided to use a special tape around the lid that could increase the isolation from the outside, because in order to place it the container always suffers slight shakes. The isolation between the outside and the inside relies solely on the lid. Every time the solution had to be changed, the lid was removed and carefully put back as to not shake the test bench.

A picture of the test bench is presented in Figure 48.

Figure 48: Picture of the test bench in the laboratory.



4.3.4 Transient Test

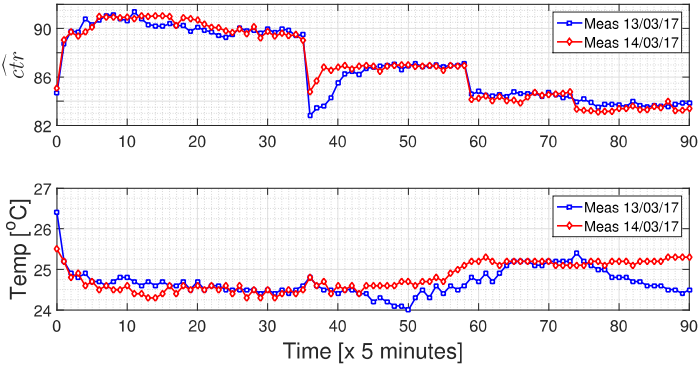
The aim of this test is to determine the amount of time it takes for the RH in the container interior to stabilize for each one of the four SSS. For this test we use TB1 supplied with V_{DDD} of 1.8 V. One frame of data is saved every 5 minutes, as well as the temperature in the outside. Each frame is processed in the function **word_value**, and the resulting array is averaged. Figure 49 present the test results for two consecutive days. The methodology for extracting these curves was:

- **At instant 0:** The $BaCl_2$ solution is put inside the container. The outside RH is 40 % for Meas 1 and 48 % for Meas 2.
- **Between instants 35 and 36:** The $BaCl_2$ solution is replaced by the NaCl solution. The outside RH is 38 % for Meas 1 and 47 % for Meas 2.
- **Between instants 58 and 59:** The NaCl solution is replaced by the $Mg(NO_3)_2$ solution. The outside RH is 42 % for Meas 1 and 44 % for Meas 2.
- **Between instants 73 and 74:** The $Mg(NO_3)_2$ solution is replaced by the $MgCl_2$ solution. The outside RH is 41 % for Meas 1 and 41 % for Meas 2.

The temperature during these tests remained within 1.5 °C of variation (excluding the first point in the first Meas). It is possible to see four distinguishable levels for the four conditions of RH. We notice a fair reproducibility between two consecutive days.

When the $BaCl_2$ solution is introduced at instant 0, it takes around 30 minutes for $\widehat{ctr}$ to converge to an approximately constant level. It is interesting to notice that $\widehat{ctr}$ first reaches one level, and after a while stabilizes in a slightly lower one. This was observed in both days. When the NaCl solution is introduced at instant 35, it takes around 50 minutes (based on the first Meas, which had the lowest external RH at the moment the container was opened) for $\widehat{ctr}$ to stabilize. For the other two SSSs it is hard to visually distinguish the time it takes to reach stabilization, first because the sensor has a lower gain in the low humidity range (<50 %), and second because the external humidity is close to the value stabilized by the SSSs. Hence, we waited for at least 1 hour for the RH to stabilize when using $Mg(NO_3)_2$ and $MgCl_2$.

Figure 49: Transient response of the measurement setup to the four reference SSSs.



It is important to notice that these transient times observed in Figure 49 represent the RH stabilization due to each SSS. The conditioner and the SAW-DL sensor responses are much faster and cannot be inferred from the present results.

4.3.5 System response to RH

The aim of this test is to obtain the system response to RH for both test board and in the two supplying conditions (V_{DDD} = 1.2 and 1.8 V). Figure 50 presents the flow chart of the methodology to obtain the results in this section. The first step is to introduce the desired SSS in the container, and wait for the RH to stabilize, based on the results obtained in the last section (Figure 49). After waiting the necessary period, we use the oscilloscope to acquire and save 10 frames of data. Each frame is processed in the **word_value** script, which returns an array with the word values. Then, we take the averages of each one of the 10 resulting arrays, which result in 10 numbers. Finally, we calculate the average and the normal standard deviation (STDV) of these 10 numbers.

Figures 51a and 51b present the measurement results of TB1 for V_{DDD} of 1.2 and 1.8 V, respectively. Each marker in this curves represent the average value obtained by applying the test methodology presented in Figure 50, and the distance between a marker and its corresponding horizontal bar repre-

Figure 50: Methodology to obtain the setup response to RH.

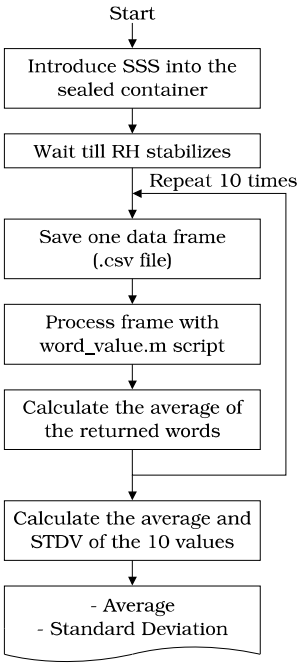


Table 12: $\widehat{ctr}$ vs RH for TB1 and V_{DDD} = 1.2 V.

	Meas 1		Meas 2	
RH [%]	**Average**	**STDV**	**Average**	**STDV**
32.8	54.61	0.1427	55.01	0.0060
52.9	55.00	0.0063	55.17	0.1444
75.3	56.53	0.3102	56.97	0.0287
90.0	57.97	0.1596	57.86	0.2275

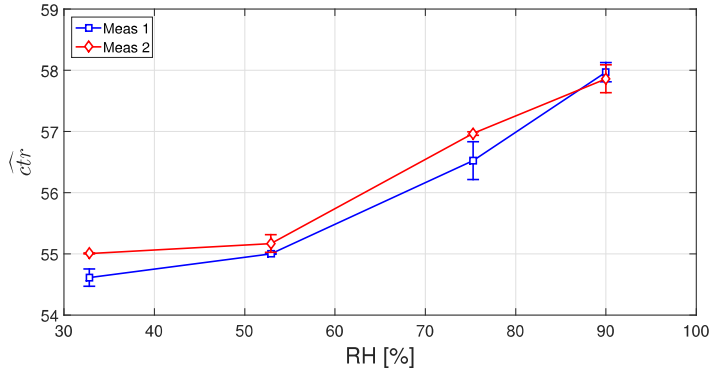
sents one STDV. The same results are presented in Tables 12 and 13. Meas 2 was obtained one day after Meas 1.

The measurement results for TB2 are presented in Figures 52a and 52b, and Tables 14 and 15. Meas 4 was obtained three days after Meas 3, and Meas 5 was obtained one week after Meas 4.

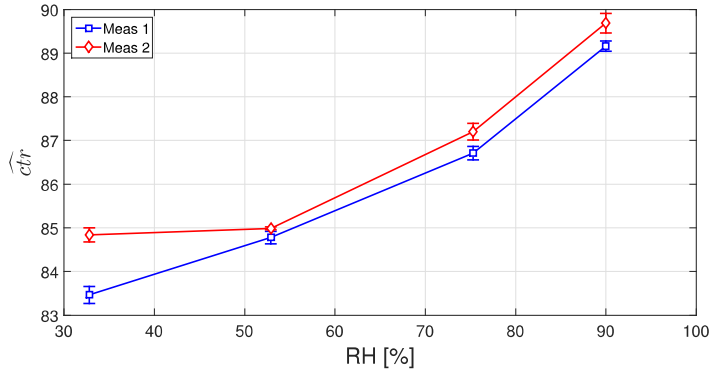
If we compare the STDVs obtained here with the ones obtained when the USRP was connected directly to the test boards, a fair reduction can be noticed. We believe one of the causes is the high quality factor (narrow-band

Figure 51: TB1 response to RH.

(a) V_{DDD} **= 1.2 V.**



(b) V_{DDD} **= 1.8 V.**

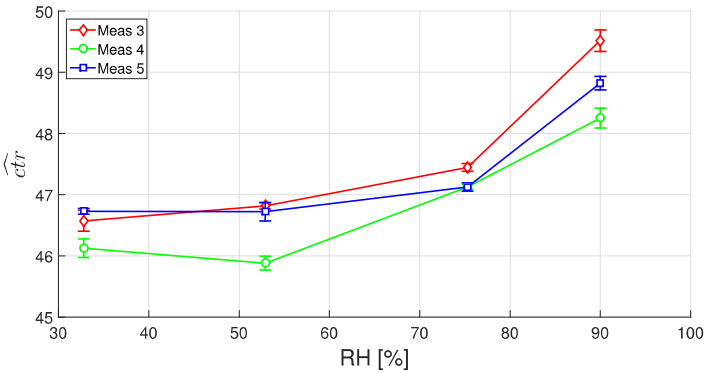


transfer function) of the SAW devices, which might be suppressing the phase-noise of the signals generated by the USRP. Since the word value is related to the phase difference between *sch* and *rch*, the phase-noise in these signals is directly converted to a noise in the output level.

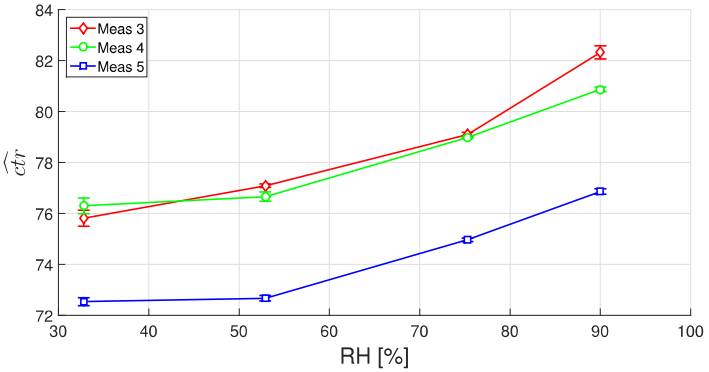
TB1 presented a monotonic increase in $\widehat{ctr}$ as a function of the RH for both supply levels. We can notice a fair reproducibility between the measurements, except for RH = 32.8 % when V_{DDD} = 1.8 V. This difference might

Figure 52: TB2 response to RH.

(a) V_{DDD} **= 1.2 V.**



(b) V_{DDD} **= 1.8 V.**



have been caused by a movement in the cables or in the setup during one of the measurements. In the range from 52.9 % to 90.0 % the responsivity of both curves is around 4.5 per RH percentage point (Figure 51b).

TB2 also presented a monotonic increase in $\widehat{ctr}$ as a function of the RH, except in Meas 4 for V_{DDD} = 1.2 V. For V_{DDD} = 1.8 V, Meas 3 and Meas 4 presented similar results, except for RH = 90 %. This difference was probably caused by a movement in the setup. Meas 5 was realized one week

Table 13: $\widehat{ctr}$ vs RH for TB1 and V_{DDD} = 1.8 V.

	Meas 1		Meas 2	
RH [%]	**Average**	**STDV**	**Average**	**STDV**
32.8	83.47	0.1925	84.84	0.1611
52.9	84.78	0.1403	84.99	0.0306
75.3	86.71	0.1545	87.20	0.1910
90.0	89.16	0.1153	89.69	0.2260

Table 14: $\widehat{ctr}$ vs RH for TB2 and V_{DDD} = 1.2 V.

	Meas 3		Meas 4		Meas 5	
RH [%]	**Average**	**STDV**	**Average**	**STDV**	**Average**	**STDV**
32.8	46.57	0.1697	46.13	0.1532	46.73	0.0479
52.9	46.82	0.0572	45.88	0.1105	46.72	0.1492
75.3	47.45	0.0641	47.13	0.0422	47.13	0.0668
90.0	49.52	0.1739	48.25	0.1614	48.82	0.1091

after Meas 4, and presents a similar variation in $\widehat{ctr}$, but with a drift in the values.

Table 16 summarizes the variations in $\widehat{ctr}$ for the five measures in the range of 32.8 to 90 % RH, for V_{DDD} = 1.8 V. An estimation of the sensing channel delay variation ($\widehat{\Delta\tau_s}$) is obtained from the DLL characterization (Table 9). The estimated sensing channel phase variation ($\widehat{\Delta\phi_{sr}}$) is also presented.

The results of the transient test (Figure 49) and of Meas 1 and 3 are the ones that are most similar in their response curves. Although Meas 2, 4, and 5 present very close values for $\widehat{ctr}$ (Table 16), their response curves have more pronounced differences.

Based on the transient test, and on Meas 1 and 3, we can estimate a variation in $\widehat{ctr}$ of around 6 for the RH in the range from 32.8 to 90.0 %. The variation in the phase of the signal applied to the SAW-DL humidity sensor

Table 15: $\widehat{ctr}$ vs RH for TB2 and V_{DDD} = 1.8 V.

	Meas 3		Meas 4		Meas 5	
RH [%]	**Average**	**STDV**	**Average**	**STDV**	**Average**	**STDV**
32.8	75.81	0.3129	76.29	0.3071	72.53	0.1616
52.9	77.08	0.0638	76.66	0.1841	72.66	0.1072
75.3	79.09	0.0955	78.98	0.0309	74.96	0.0734
90.0	82.31	0.2553	80.86	0.0895	76.85	0.1058

Table 16: Summary of the humidity test results for both test boards and V_{DDD} = 1.8 V.

	TB1		TB2		
	Meas 1	**Meas 2**	**Meas 3**	**Meas 4**	**Meas 5**
$\Delta\,\widehat{ctr}$	4.85	5.69	6.50	4.57	4.32
$\widehat{\Delta\tau_s}$ **[ps]**	190.56	223.56	264.35	185.86	175.69
$\widehat{\Delta\phi_{sr}}$ [°]	10.98	12.88	15.23	10.71	10.12

was around 15° in the tested RH range.

4.3.6 Conclusions of the humidity tests

The novel conditioner for SAW-DL sensors proposed and designed in this work was tested with a SAW-DL humidity sensor. The data obtained with our measurement setup demonstrates that the system responds to RH roughly as expected. We were able to measure RH in a range from 32.8 to 90 %. Four distinguishable levels can be noticed for the four RH conditions (see Figure 49). The results were fairly reproduced between two consecutive days. We estimate a variation of around 6 in the conditioner output word value for the tested RH range, which, based on the DLL characterization, translates to a variation of around 15° in the phase of the electric signal applied to the SAW-DL humidity sensor.

The test setup was not the ideal for delay measurements, mainly because the parts were connected with cables. Small movement in the test bench might significantly alter the results, specially in this case where we are measuring time-delays in the order of picoseconds. If two RH measurements are realized with one week apart from each other, as for Meas 4 and Meas 5 of TB2, we hypothesize that the drift in the word value vs RH curve appears because of small movements in the setup[7]. This effect can also be responsible, or at least contribute, to small drifts in the curves between two consecutive days.

Other possible contributor for the drifts between the curves is a permanent or casual leakage in the container. If the interior is not completely sealed, the external humidity may influence the internal RH. Temperature differences may also be contributing to the drifts. The temperatures registered during the humidity tests (Tables 22 and 23) only served to control high fluctuations,

[7]It is virtually impossible to avoid movements in the setup throughout a whole week.

but they do not represent the actual temperature in the container interior at the moment of each acquisition. Finally, the unexpected behavior in the DLL curves (see Figures 44 and 45) caused by a wrong transition in the flag signal *up* may also be contributing to the drifts in the humidity measurement curves.

In order to obtain a more robust setup, the SAW devices, the IC, and the reference signal generator should be mounted on the same PCB, which would avoid the use of cables. By doing so, we believe variations between the measurements of the same RH condition will be greatly reduced. The data acquisition and processing can also be improved by continuously sampling the data, and by taking the averages in wider data windows. In our measurements the data window was limited to the size the oscilloscope could properly save.

5 CONCLUSIONS

In this work we proposed, designed, and tested a novel conditioner for general SAW-DL sensors. The main idea behind this novel architecture is to use the SAW-DL sensor in open loop configuration, and measure the time-delay added in a reference signal applied to it with a Delay-Locked Loop. This delay can be made sensitive to a wide variety of physical, chemical, and biological quantities by proper designing the SAW-DL sensor, as the literature in the area has extensively demonstrated. The DLL is employed in the proposed conditioner to make the conversion of delay to a voltage level, or, in the case of our implementation, to a digital word.

This direct conversion of the measurand to a digital word is the main advantage of the proposed conditioner. The standard measurement setups in the literature require expensive and large electronic equipments such as a spectrum analyzer, a vector network analyzer, or a frequency counter. This is not the case for our system. Although the measurements presented in this work required an oscilloscope for data acquisition, the digital word can be acquired and better processed in a cheap, off the shelf microcontroller.

The conditioner was designed in the technology GF CMOS 130 nm, available to us through the educational program of MOSIS. We adopted a fully-digital architecture, which has the well-known advantages of low-area and low-power consumption. Except for the input comparators, the designed system is entirely composed of standard logic circuits, which makes it easier to transition to other technology nodes. The output is a serial digital word which can be acquired and processed in a microcontroller or computer. During the design, special care was taken in order to facilitate testing and debugging. It is possible to open the DLL loop and apply an external control word, which allows the characterization of the DCDL stand-alone. A test multiplexer was also included, allowing the measurement of eight internal signals.

Although the fully-digital DLL architecture used in this work is not a novelty, it is the first time this system is used in the conditioning of a SAW-DL sensor[1]. Moreover, the implementation of the DCDL is completely new, and has the advantage of only using standard logic, avoiding the use of RF filters, varactors, or current starving structures. For these reasons, this block presents a good linear response of delay versus the applied control word. Therefore, the proposed DCDL might be applicable in other DLL applications, such as

[1] To the best knowledge of the authors.

data and clock recovery.

The first part of the measurement comprised the tests of the conditioner stand-alone. In this tests we detected a problem concerning the accumulator. This issue reflects in a discontinuity in the central point of the DLL response curve. Fortunately, this problem did not prevent the rest of the measurements. It is important to say that this malfunctioning can be fixed in future designs, and do not invalidate any ideas or results. All the other functions that we were able to test behaved as expected.

The SAW devices used as reference and sensing channels were fixed in the walls of a sealed container. Four saturated saline solutions were used to stabilize the container interior to four distinct RH levels. The reference signal was generated by a USRP board, and coupled to the SAW devices via coaxial cables. The test board, which contains the designed conditioner, was also coupled to the SAW devices via coaxial cables.

The measurements show a distinct variation in the mean value of the output word for each level of RH, specially in the range of 50 to 90 % RH. In order to increase the responsivity of the system to RH, the core voltage V_{DDD} was increased from 1.2 to 1.8 V in some tests. This increment boosts the DCDL by decreasing the delay step δ. The result is a larger variation in the output word for the same variation in RH. The four RH conditions were replicated and measured several times, with intervals of one to seven days between each measurement. We noticed a fair reproducibility between the measurements of consecutive days. When comparing two measurements with one week apart from each other, we notice a drift in the curves. This is a result of movements in the setup that could not be avoided throughout a whole week.

The humidity measurements were affected by the coaxial cables that connect the USRP board, the SAW devices, and the test boards. Since we are measuring delays in the order of picoseconds, movements in the setup can reflect in unintended variations in the output word. When we detected this problem, the SAW devices were already fixed in the container, and remove them could compromise their operation. Therefore, we used rigid coaxial cables, fixed the container and the cables in the table, and tried to avoid hitting or shaking the setup (which is not as easy as it seems). However, for future prototypes the best solution is to integrate the reference signal generator, the SAW devices, and the conditioner circuitry in the same PCB.

To conclude, we were able to demonstrate the operation of the proposed conditioner for a SAW-DL humidity sensor. Although the setup can have a lot of improvement, the data obtained validates its ability to discriminate

Table 17: Comparision with the selected research

	(PENZA; CASSANO, 2000)	(BORRERO *et al.*, 2013)	(RAJ *et al.*, 2013)	(CAI *et al.*, 2015)	**This Work**
Type of SAW sensor	Delay Line	Resonator	Resonator	Resonator	**Delay Line**
Operating Frequency	468 MHz	65 MHz	433.9 MHz	6.4 GHz (3rd harm)	**160 MHz**
Measurand	Relative Humidity	Pressure, Temperature, Impedance	Chemical Warfare Agents	Mouse cancer cells and DNA bases	**Relative Humidity**
Output Format	Frequency	Reflection Coefficient	Frequency	Reflection Coefficient	**Time-Delay**
Required Equipments	Frequency Counter + PC	VNA	SA	VNA	**PC**

RH levels. Table 17 presents a comparision of this work with the selected research presented in Section 1.2.

5.1 RECOMMENDED IMPROVEMENTS FOR FUTURE DESIGN

- The *up* signal must be registered in a way to avoid it transitions during a falling edge of *clk*, in order to avoid the undesired jumps observed in the response of the DLL when the control word value is close to 64.
- The DCDL can be drastically reduced, since only a short range is used to track the delay variations in the SAW-DL sensor case study. A mechanism of phase-compensation has to be designed in order to calibrate each conditioner. This mechanism can be made externally with passive components, for instance, to avoid power consumption.
- The power consumption can be strongly reduced, specially in the input comparators.
- The P2S block could be compatible to a data exchange protocol (like SPI, or I2C) to ease the communication with a microcontroller.
- A better design of the inverter and of the delay element could lead to a smaller δ, which would in turn increase the gain of the DLL.
- The reference signal generator, the SAW devices, and the conditioner circuitry must be integrated in the same PCB. The connection of these blocks with coaxial cables must be avoided, since we are measuring delays. Movements in the cables are suspected to be producing unintended response.

- It might be better to connect the input of the frequency divider to the reference channel (*rch*), since it will not vary with the measurand.
- The reference and sensing devices should be fabricated on the same substrate in order to improve the system immunity to temperature variations.

5.2 TOPICS FOR FUTURE WORKS

- To study the dynamics and non-linearities of the system. It might be necessary to better understand the dynamics if the interaction of the measurand with the sensor surface is faster.
- Model the digital system in VHDL.
- Continuously acquire the output words in a microcontroller, and take the average in a larger window to have a more stable data.
- Measure the system in a more controllable environment. Preferably in a chamber where the temperature and humidity can be precisely controlled.

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APPENDIX A – CODES AND SCRIPTS

A.1 DE0-NANO VERILOG CODE

This section presents the Verilog code installed in the DE0-Nano board. This code serves to synchronize the edges of the reset signal generated in pin **P4** with the clock signal in pin **P0**, and also to buffer the output signal. The mapping of the test board pins to the DE0-Nano board is: pin **P0** is connected to pin addressed to input **clk_i**, **P1** to input **data_i**, **P4** to input **rst_i**, and **P2** to output **rst_out**. Channel 1 of the oscilloscope is connected to pin addressed to output **clk_o**, channel 2 to **data_o**, and channel 3 to **rst_o**.

```
module sensor
  (
    input data_i,
    input clk_i,
    input rst_i,

    output reg rst_out,
    output clk_o,
    output data_o,
    output rst_o
  );

always @(negedge clk_i) begin
    rst_out = rst_i;
end

assign clk_o = clk_i;
assign data_o = data_i;
assign rst_o = rst_out;

endmodule
```

A.2 WORD VALUES

An Octave function was developed in order to decode the output data stream. This function is presented below and is called **word_value**. An example of data processed by this function is presented in Figure 53. Channel 1 of the oscilloscope measures the clock signal, which is also used to pace the P2S converter. Channel 2 measures the output data stream, and channel 3 the reset signal. The data is saved in a csv file whose first column is time, second is the clock signal, third the output stream, and forth the reset signal. This file is loaded to matrix **data**, and passed to the function **word_value**. Additionally, we have to pass the threshold voltage **vth** (1.65 V), and the initial point to output (in order to disregard the initial transient). If we apply the data presented in Figure 53 to this function, the result is the one presented in Figure 54 (**initial_point** was set to 1).

```
function value = word_value(data,vth,initial_point)

%%%% "data" is a matrix whose columns are: time, clk, out_stream
    , reset

kk = 1;

while data(kk,4) >= vth % while reset is high

    kk=kk+1;

end

data = data(kk:length(data(:,1)),:); % removes the data previous
    to the falling edge of reset

lgth = length(data(:,1));

for ii=1:lgth % maps the out_stream logic high to 1, and logic
    low to 0

    if data(ii,3) > vth

        data(ii,3) = 1;

    else

        data(ii,3) = 0;

    end

```

```
29  end
30
31  jj=1;
32
33  for ii=2:lgth % finds all the falling edges of clk, which is
        where the out_stream will be sampled
34
35      if (data(ii,2) < vth) && (data(ii-1,2) >= vth)
36
37          points(jj) = data(ii-1,3);
38
39          jj = jj+1;
40
41      end
42
43  end
44
45  num = floor((jj-1)/8); % finds the number of 8-bits packages
        contained in the out_stream
46
47  for ii=0:(num-1) % samples the data, and converts the binary 7-
        bits word of each pakage into its decimal value
48
49      value(ii+1) = (2^6)*points(8*ii+1)+(2^5)*points(8*ii+2) ...
50          +(2^4)*points(8*ii+3)+(2^3)*points(8*ii+4) ...
51          +(2^2)*points(8*ii+5)+(2^1)*points(8*ii+6) ...
52          +(2^0)*points(8*ii+7);
53
54      if points(8*ii+8) ~= 0 % checks if the 8th bit of each
            package is indeed 0
55
56          error('Error: wrong end bit');
57
58      end
59
60  end
61
62  value = value(initial_point:end); % returns an array with the
        successive word values contained in out_stream
63
64  end
```

Figure 53: Example of data frame acquired in the oscilloscope.

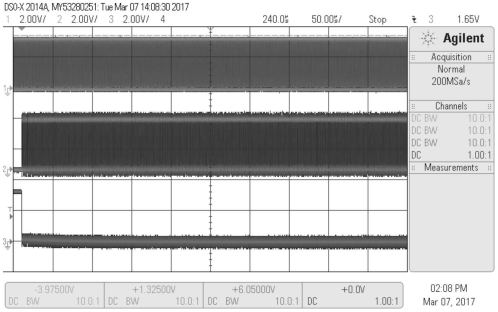
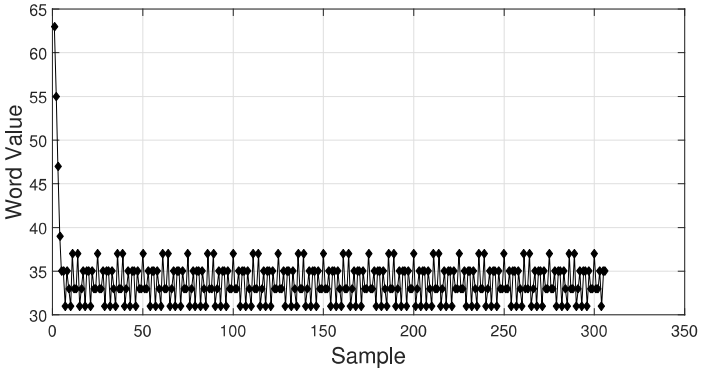


Figure 54: Example of word_value solution.



APPENDIX B – ADDITIONAL TEST RESULTS

B.1 USRP OUTPUT POWER

The output power of the USRP board ports was measured with a spectrum analyzer (SA) in order to determine the relationship between the variable "gain" and the actual power delivered to the load for a signal of 160 MHz. The SA is a N9913A of Agilent Technologies, with 50 Ω of input impedance. One of the ports of the USRP board was connected to the input of the SA, while the other was terminated with a 50 Ω load. Figure 55 presents the measurement results for channel A and B, and for three values of "gain": 30, 40, and 50. Therefore, the relationship between the power delivered to a 50 Ω load and variable "gain" can be expressed as P_{dBm} = "gain" - 64.2[1].

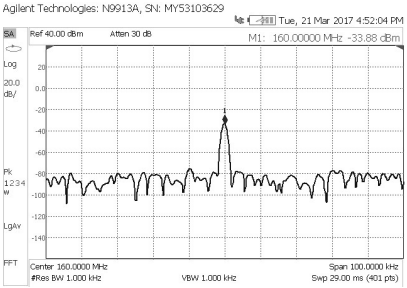
B.2 DLL CURVES AVERAGES AND STANDARD DEVIATIONS

The average values and standard deviations of the curves 44a, 44b, 45a, and 45b are presented, respectively, in Tables 18, 19, 20, and 21.

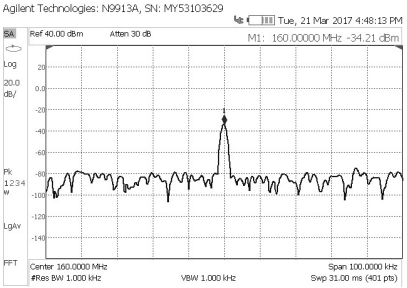
[1] By taking the average value of the two channels for each value of "gain" and then applying it to a linear regression tool.

Figure 55: USRP board output power.

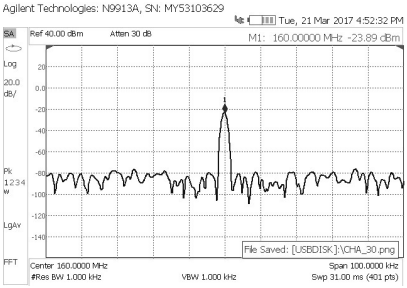
(a) Channel A, "gain" = 30.



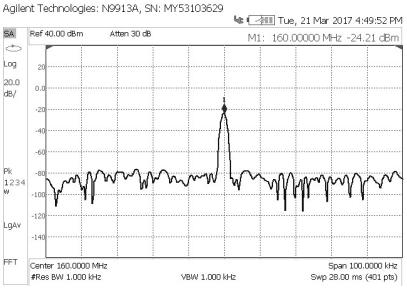
(b) Channel B, "gain" = 30.



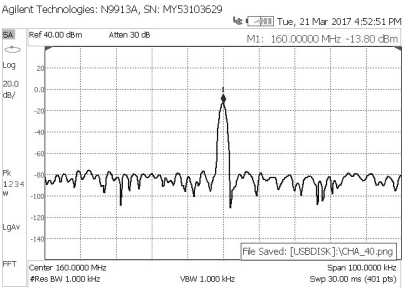
(c) Channel A, "gain" = 40.



(d) Channel B, "gain" = 40.



(e) Channel A, "gain" = 50.



(f) Channel B, "gain" = 50.

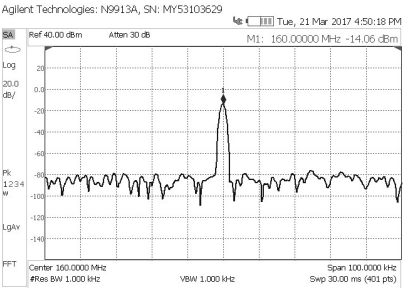


Table 18: DLL curve for TB1 and V_{DDD} = 1.2 V.

Phase [π rad]	Average	STDEV	MIN	MAX
-0.40	18.085	0.118	17.856	18.245
-0.30	23.337	0.261	22.984	23.903
-0.20	28.602	0.226	28.245	28.891
-0.10	33.706	0.330	33.226	34.471
0.00	38.895	0.254	38.183	39.000
0.10	43.925	0.110	43.778	44.136
0.20	48.627	0.157	48.432	48.922
0.30	53.820	0.227	53.529	54.105
0.40	59.030	0.448	58.572	59.716
0.50	61.415	0.362	60.914	62.136
0.50	127.000	0.000	127.000	127.000
0.60	66.547	0.383	65.809	66.977
0.60	69.506	0.327	68.844	69.848
0.70	74.788	0.122	74.689	75.062
0.80	79.798	0.133	79.529	79.973
0.90	84.846	0.403	84.424	85.669
1.00	90.453	0.515	89.669	91.000
1.10	95.992	0.388	95.529	96.712
1.20	100.780	0.185	100.500	101.100
1.30	105.930	0.336	105.540	106.650
1.40	111.130	0.201	110.840	111.420
1.50	116.290	0.602	115.090	116.910

Table 19: DLL curve for TB1 and V_{DDD} = 1.8 V.

Phase [π rad]	Average	STDEV	MIN	MAX
-0.70	5.209	0.335	4.611	5.607
-0.60	9.599	0.374	9.093	10.300
-0.50	17.441	0.305	16.977	17.895
-0.40	24.987	0.228	24.626	25.311
-0.30	33.142	0.482	32.603	33.911
-0.20	41.002	0.383	40.533	41.490
-0.10	48.612	0.390	47.981	49.374
0.00	56.995	0.362	56.237	57.444
0.10	60.761	0.455	60.066	61.436
0.10	69.318	2.770	65.342	74.969
0.20	69.184	0.358	68.875	70.058
0.20	72.922	0.331	72.331	73.420
0.30	80.681	0.360	80.268	81.467
0.40	88.505	0.336	87.988	89.016
0.50	96.961	0.363	96.432	97.475
0.60	104.810	0.366	104.290	105.440
0.70	112.690	0.400	112.030	113.290
0.80	120.680	0.301	120.330	121.260

Table 20: DLL curve for TB2 and V_{DDD} = 1.2 V.

Phase [π rad]	Average	STDEV	MIN	MAX
-0.30	15.978	0.814	15.023	17.000
-0.20	18.913	0.374	18.268	19.350
-0.10	24.128	0.375	23.296	24.588
0.00	29.217	0.123	29.039	29.397
0.10	34.894	0.319	34.105	35.249
0.20	39.802	0.265	39.265	40.206
0.30	44.571	0.442	43.490	44.961
0.40	48.724	0.242	48.253	49.093
0.50	53.690	0.308	53.319	54.292
0.60	58.780	0.188	58.564	59.086
0.70	72.414	9.002	61.420	79.591
0.70	65.685	0.270	65.148	65.957
0.80	71.077	0.202	70.782	71.311
0.90	76.047	0.213	75.700	76.377
1.00	80.369	0.345	79.879	80.821
1.10	85.332	0.189	85.093	85.615
1.20	90.563	0.322	90.066	91.179
1.30	95.981	0.533	95.374	96.977
1.40	101.000	0.308	100.640	101.560
1.50	105.630	0.253	105.370	106.100
1.60	110.440	0.430	109.590	111.000
1.70	112.090	0.265	111.820	112.660

Table 21: DLL curve for TB2 and V_{DDD} = 1.8 V.

Phase [π rad]	Average	STDEV	MIN	MAX
-0.55	4.587	0.436	3.794	5.016
-0.50	8.107	0.120	7.833	8.261
-0.40	15.207	0.186	15.000	15.591
-0.30	21.497	0.453	20.696	22.128
-0.20	29.094	0.445	28.160	29.700
-0.10	37.399	0.325	36.922	37.911
0.00	44.695	0.447	44.082	45.490
0.10	51.484	0.204	51.249	51.825
0.20	58.823	0.362	58.300	59.405
0.25	65.704	1.834	63.770	69.296
0.30	68.493	1.391	66.953	72.198
0.35	71.851	0.472	70.821	72.300
0.40	75.342	0.546	74.222	75.981
0.50	82.447	0.519	81.514	83.093
0.60	90.120	0.556	89.070	91.000
0.70	98.926	0.616	97.482	99.537
0.80	107.250	0.224	106.910	107.590
0.90	115.190	0.746	113.680	116.060
1.00	124.230	0.316	123.580	124.710

B.3 TEMPERATURE DURING HUMIDITY TESTS

The temperatures during the humidity tests (Section 4.3.5) are presented in Tables 22 and 23.

Table 22: Temperatures during TB1 humidity tests.

	Meas 1		**Meas 2**	
	1.2 V	**1.8 V**	**1.2 V**	**1.8 V**
$MgCl_2$	25.1	25.3	24.9	24.7
$Mg(NO_3)_2$	25.1	25.1	24.7	24.6
NaCl	24.5	24.4	24.4	24.5
$BaCl_2$	25.1	25.0	24.4	24.3

Table 23: Temperatures during TB2 humidity tests.

	Meas 3		**Meas 4**		**Meas 5**	
	1.2 V	**1.8 V**	**1.2 V**	**1.8 V**	**1.2 V**	**1.8 V**
$MgCl_2$	25.6	25.4	25.4	26.0	25.9	26.2
$Mg(NO_3)_2$	26.2	26.2	25.5	25.6	26.0	25.8
NaCl	26.0	25.9	24.6	24.0	26.1	26.1
$BaCl_2$	25.6	25.7	23.9	23.7	26.0	26.1

APPENDIX C – LAYOUTS

This Appendix presents the layout views of the blocks that compose the system.

Figure 56: Layout of the combinational logic circuits.

(a) NOT **(b) 2-NAND** **(c) 2-NOR**

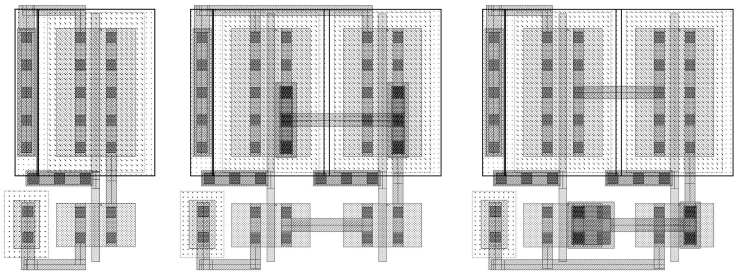


Figure 57: Layout of the D flip-flop with asynchronous preset and reset.

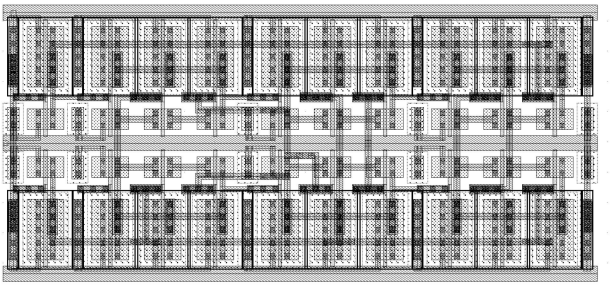


Figure 58: Layout of the 8:1 multiplexer.

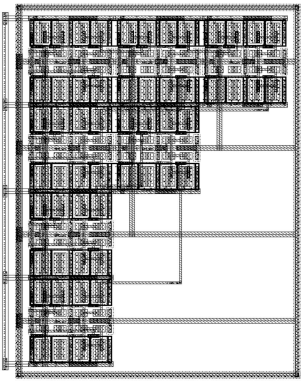


Figure 59: Layout of the three-state swith with non-inverted control.

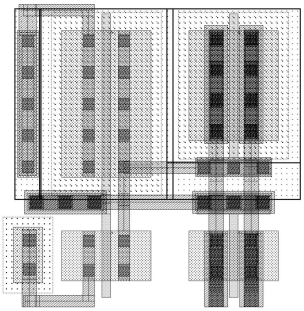


Figure 60: Layout of the level shifters (not in the same scale).

(a) DLS **(b) ULS**

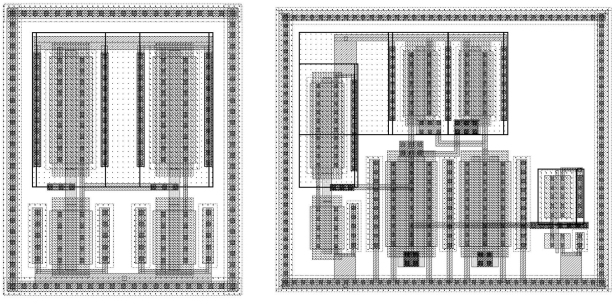
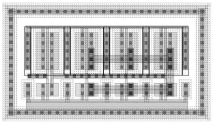


Figure 61: Layout of the buffers (not in the same scale).

(a) Inverter chain with 2 inverters



(b) Inverter chain with 4 inverters.

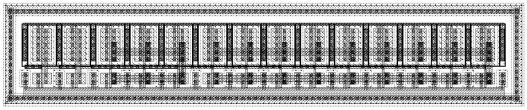


Figure 62: Layout of the frequency divider.

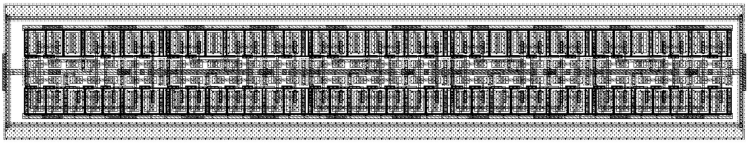
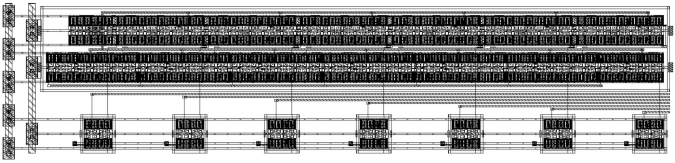


Figure 63: Layout of the 7-bits accumulator.

(a)



(b)

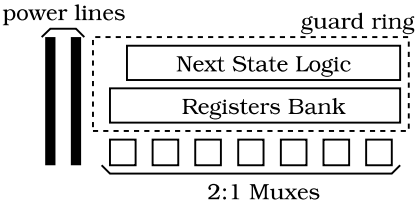
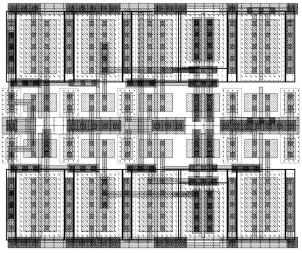


Figure 64: Layout of the delay element.

(a)



(b)

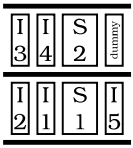
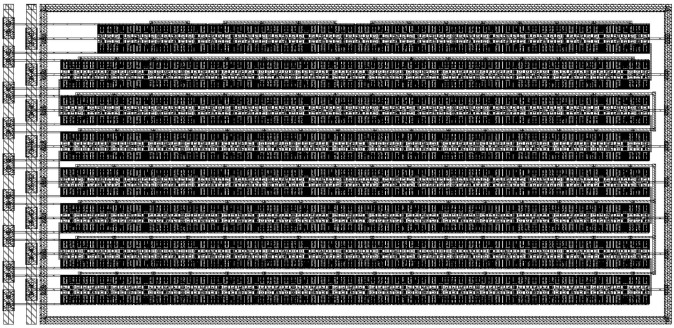
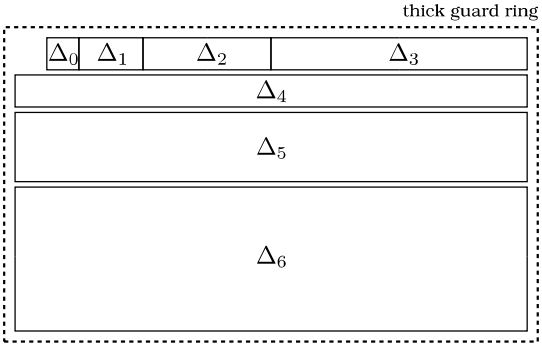


Figure 65: Layout of the DCDL.

(a) Layout



(b) Floorplan



(c) Power distribution network (thick) and signal flow (dashed)

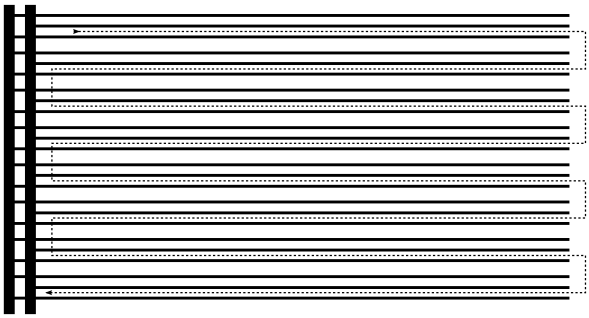


Figure 66: Layout of the input comparator.

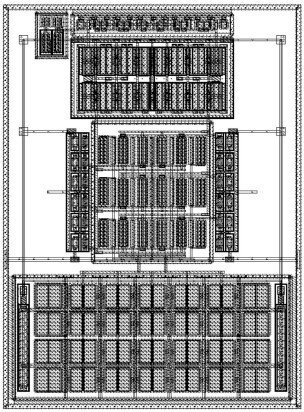


Figure 67: Layout of the parallel-to-serial converter.